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A constrained optimization approach for accurate and area efficient bandgap reference design

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ABSTRACT

In this paper, a constrained optimization approach for the design of bandgap reference (BGR) circuits that meet a given voltage inaccuracy specification while minimizing area is presented. Device matching properties and error propagation analysis are carried out such that the desired performance can be achieved by the optimization algorithm. The BGR occupies 0.097 mm^2 in a 0.35 μm CMOS process. Experimental results verified the effectiveness of the optimization algorithm by producing a voltage reference of 1.220 V, with a relative inaccuracy ($3\sigma/\mu$) of 0.65% at 27 °C and TC = 13.7 ppm/°C in the range of − 10 °C to 125 °C, for all 40 fabricated samples, without trimming. Also shown in the paper and verified experimentally, a 3-fold reduction in inaccuracy, to 0.20% at 27 °C, can further be obtained, if needed, by a simple one-temperature four-bit trimming.

1. Introduction

Bandgap reference (BGR) circuits are designed with the purpose of generating on chip a voltage or current that shows, for a given application, sufficiently low sensitivity to process variations and device mismatch, and low temperature drift, while meeting other demanding performance requirements in integrated circuit designs, such as small area and low power consumption. Area reduction can be achieved in advanced technology nodes, as in nanometer-scale circuit designs, which are, however, subject to a wide range of effects that are manifested as large parameter variations and device mismatch [1]. In order to improve the accuracy of BGRs, temperature trimming schemes have been applied [2–4], which usually require a relatively large number of trimming bits, thereby increasing power consumption, circuit area, and manufacturing cost owing to the additional post-fabrication procedure. Other approaches include curvature compensation [5,6,8], design of operational amplifiers employing correlated double sampling [9] or chopping techniques [3] to reduce offset voltage caused by device mismatch. In such cases, the benefits are obtained at the expense of circuit area and/or power consumption increase. In [10] resistors were replaced by a bipolar transistor and additional circuitry to enable operation at very low power consumption. Large inaccuracy and temperature coefficient (TC) resulted as consequences.

In view of the potential to exploit design trends favoring BGRs, alternative approaches whereby accuracy is improved by proper design sizing have been reported [11,12]. However, in [11] no optimization strategy is presented to relate circuit area and acccuracy, and in [12] device sizing is carried out through a heuristic approach, which leads to sub-optimum solutions.

In this work a constrained optimization method is proposed to design a BGR circuit which requires the minimum die area that meets a given accuracy specification for its reference voltage. Consequently, this paper advances a design technique that combines device-matching properties [13] and error propagation analysis [14] to develop an algorithm that minimizes the BGR circuit area, while ensuring the specified voltage accuracy defined by the circuit designer. Section 2 presents the BGR circuit analysis and describes the design approach. Section 3 develops the optimization methodology. Section 4 shows measurement results and Section 5 concludes the paper.

2. Bandgap reference structure

A BGR can be designed according to the block diagram shown in Fig. 1, where a voltage V_{REF} that is practically independent of temperature is produced by adding a negative TC voltage V_{EB_2} to a positive TC voltage ΔV_{EB}, that is,

$$V_{REF} = V_{EB_2} + C\Delta V_{EB}, \tag{1}$$

and C is a temperature-independent constant weighting factor. The corresponding circuit can be realized using the traditional structure in Fig. 2(a), where $\Delta V_{EB} = V_{EB_1} - V_{EB_2}$, and the start-up circuit in Fig. 2(b).

Assuming ideal operational amplifier (OTA), identical transistors M_1

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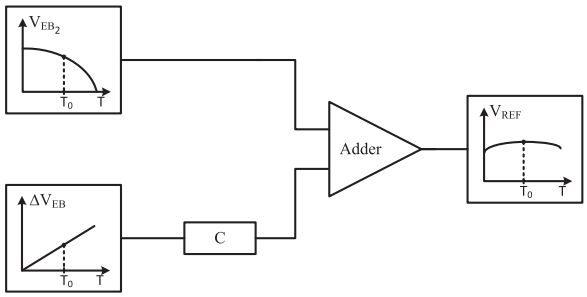

Fig. 1. Block diagram of the bandgap reference.

and M_2, and $n + 1$ identical BJTs, we write

$$I_1 = I_2 = \frac{\Delta V_{EB}}{R_1} = \frac{V_T \ln(n)}{R_1}, \tag{2}$$

where V_T is the thermal voltage that has a proportional-to-absolute-temperature (PTAT) behavior. The reference voltage can thus be written as

$$V_{REF} = V_{EB_2} + V_T\left(\frac{R_2}{R_1} + 1\right)\ln(n), \tag{3}$$

where R_2/R_1 and n are determined such that V_{REF} becomes nearly independent of temperature over the range of interest.

2.1. Amplifier design

A simple amplifier structure was chosen in order to reduce power consumption and offset voltage. Presented in Fig. 3, the amplifier was designed with the differential pair $M_8 - M_9$ operating in weak inversion. A PTAT bias current of 400 nA through M_7 is provided by the BGR by means of M_1, M_2, M_3, and M_6. The offset voltage V_{OS} in Fig. 4 comprises systematic and random component mismatch. The former, produced by channel length modulation effects in M_4 and M_5, is reduced by choosing the same dimensions for M_3, M_4, and M_5, whose lengths are equal to those of M_1 and M_2 [15]. The latter results from mismatches between M_4 and M_5 and between M_8 and M_9, and is minimized by the optimization algorithm described in Section 3.

2.2. Number of BJTs

Taking into account the offset voltage, the reference voltage (3) becomes

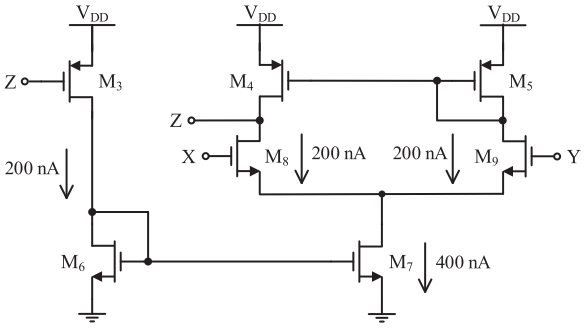

Fig. 3. Amplifier schematic diagram: M_8 and M_9 operate in weak inversion.

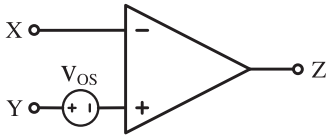

Fig. 4. Amplifier offset.

$$V_{REF} = V_T \ln\left(\frac{\Delta V_{EB}}{nR_1 I_S}\right) + \left(\frac{R_2}{R_1} + 1\right)\Delta V_{EB}, \tag{4}$$

where

$$\Delta V_{EB} = V_T \ln(n) + V_{OS}. \tag{5}$$

The product $(R_2/R_1 + 1)\ln(n)$ in (3) establishes the combination of CTAT and PTAT voltages such that $dV_{REF}/dT = 0$ at a given $T = T_0$, around which the dependence of V_{REF} on temperature is minimized. Therefore, an increase of n requires a decrease of the ratio R_2/R_1, and both reduce the influence of V_{OS} on V_{REF}, as indicated by (4) and (5)). Evaluations of trade-offs involving (i) the influence of V_{OS} on V_{REF}, (ii) the relatively large area occupied by the BJTs (each BJT has a fixed emiter area of 10 μm x 10 μm in 0.35 μm CMOS process), and (iii) the effects of systematic and random mismatching on the BJTs [16], lead to $n = 24$, so that $Q_1, Q_2, \ldots, Q_{25}$ could be arranged as a 5×5 matrix, having Q_1 placed at the center in a common centroid geometry, thereby reducing process gradient effects.

Listed in Table 1, the W/L ratios of the amplifier devices and the resistor values were determined from the above considerations. The optimization algorithm thus finds the device dimensions that minimize the total area, subject to the device parameter values in Table 1 and to a given accuracy specification of the reference voltage.

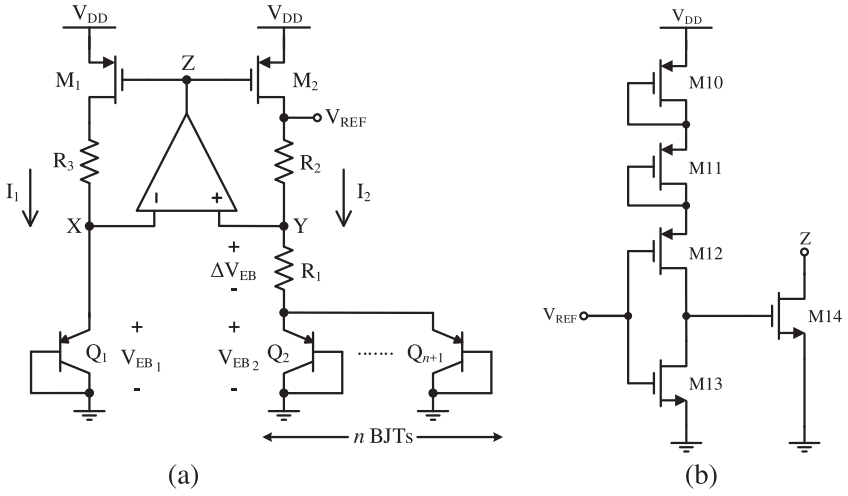

Fig. 2. Bandgap reference (a) and start-up (b) circuit diagrams.