Analog CMOS implementation of FFT using cascode current mirror

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ABSTRACT

Discrete Fourier Transform plays a vital role in the field of Digital Signal Processing. Fast Fourier Transform is an efficient algorithm to compute Discrete Fourier Transform. A novel method for the analog CMOS implementation of FFT using cascode current mirror is proposed. FFT is implemented using simple and cascode current mirrors and the results are compared for real and complex inputs. The proposed method gives more accurate results than that using simple current mirrors. The circuit implementation is rigorously verified for 4-point and 8-point FFTs. Simulation was done using Micro-Cap 10. The proposed method offers better accuracy for higher point FFTs.

1. Introduction

The Fast Fourier Transform (FFT) is a widely used signal processing and analysis concept. Availability of special purpose hardware in both commercial and military sectors has led to sophisticated signal processing systems based on the features of the FFT [1,10]. High speed data communication methods like Orthogonal Frequency Division Multiplexing (OFDM) requires highly efficient Fast Fourier Transform (FFT)/Inverse FFT (IFFT) processors for achieving superior performance. Different algorithms are available for the computation of FFT, among which, the Cooley–Tuckey algorithm is widely used [1]. The main operations involved in calculating FFT are addition and multiplication only. Analog FFT can be useful in combination with analog decoder for OFDM systems [3,10]. FFT implementation in analog domain [3–5] is cost effective and faster compared to digital implementation. In analog domain, summing does not need any additional circuitry whereas in digital domain FFT implementation needs extra adders. Current mirror circuits [6,7] can effectively implement analog FFTs with much lesser complexity. A number of works have been reported which implement FFT using simple current mirror [3,4,8]. Previous works include implementation of FFT using full radix and split radix [3,8]. Since, radix-2 implementation is simpler than other radix operations, radix-2 implementation is adopted in this paper. An Analog/ Mixed-signal (AMS) FFT circuit topology which significantly reduces the power consumption in the OFDM systems is reported in [9].

In this paper, Analog radix-2 FFT implementation using CMOS cascode current mirror is proposed. The weakness of simple current mirror in copying current is overcome by using cascode current mirror. It is the understanding of this author that eventhough there are works that implemented FFT using current mirrors, none of the works discussed the reliability issues such as hot carrier injection (HCI). The proposed method is novel in the sense that it implements FFT using cascode current mirror with high output impedance instead of simple current mirror, incorporating the method to counterbalance the reliability issues. SASP based full software radio which implements FFT by using voltage samples on the capacitor has also been reported [11, 12]. Design of charge domain DFT filter, CRAFT, based on passive switched capacitors is described in [13–15]. But in the proposed method, instead of addition of voltage samples, current addition is done and only CMOS transistors and connecting wires are required to perform FFT operation and require no passive components or additional adders or multipliers which inherently attenuate the signal. Thus require less die area than previous works. Since current mode circuit is used, parasitic effects of wires are negligible. Proposed method gives accurate result compared to previous works [3,8] that implemented FFT using simple current mirror and simulation data verifies the result.

The organization of the paper is as follows. Section 2 explains the principles of FFT, simple current mirror and cascode current mirror in detail. Section 3 discusses the analog implementation of 4-point and 8-point FFTs using simple and cascode current mirrors and the corresponding circuit simulations. Section 4 describes the simulation results of the simple current mirror implementation and proposed FFT implementation. Section **5 discusses Key parameters and reliability considerations** , Section **6** contains comparison of the results with previous work. Finally, Section 7 concludes the result.

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2. Basic principles

2.1. Fast Fourier Transform (FFT)

FFT is an efficient algorithm to find Discrete Fourier Transform (DFT). This algorithm is based on the successive decomposition of an N-point DFT into smaller DFTs. DFT of a discrete sequence $x[n]$ can be expressed as

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{nk} \tag{1}$$

for $k = 0, 1, 2, \ldots (N-1)$, where $W_N = e^{-j2\pi/N}$ is the twiddle factor. The direct computation of DFT for each value of $X[k]$ need N complex multiplication and $(N-1)$ complex additions. To compute all N values of $X[k]$, for $n = 0, 1, 2, \ldots (N-1)$, we need N^2 complex multiplications and $N(N-1)$ complex additions. Computational complexity of DFT is $\propto N^2$. So direct implementation of DFT is not efficient. FFT reduces the complexity to an order of $N \log_r N$, where r is the radix of the FFT algorithm. It explores the symmetry property and periodic property of the twiddle factors:

Symmetry Property: $W_N^{k+N/2} = -W_N^k$

Periodicity Property: $W_N^{k+N} = W_N^k$

There are 2 types of FFT algorithms, according to Cooley–Tuckey [2]: Decimation In Time (DIT) and Decimation In Frequency (DIF). This paper deals with DIT algorithm. The radix-2 DIT algorithm rearranges the DFT equation into two parts: a sum over the $\frac{N}{2}$ even numbered discrete-time indices ($n = 0, 2, 4, \ldots (N-2)$) and a sum over the odd numbered indices ($n = 1, 3, 5, \ldots (N-1)$):

$$X[k] = \sum_{n=0}^{N/2-1} x[2n] W_N^{2nk} + \sum_{n=0}^{N/2-1} x[2n+1] W_N^{(2n+1)k} \tag{2}$$

This algorithm is named as DIT, due to the splitting of the time domain sequence into even and odd samples as in Eq. (2).

2.2. Current mirror

The current mirror is used in circuits to provide bias currents to other parts of the circuit [6,7]. A simple current mirror contains two active devices and the current through one is controlled by current through the other. That is, current mirror is used to replicate the current in a circuit. Fig. 1 shows a simple current mirror circuit with two active devices M_1 and M_2. The drain of transistor M_1 is shorted to its gate, so that it is operating in saturation region. In order to work the current mirror properly, M_2 must also be in saturation. The drain currents can
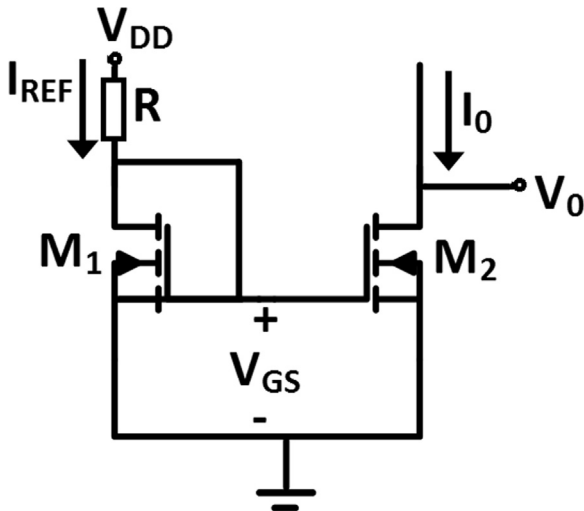
be expressed as

$$I_{REF} = \frac{1}{2} K'_n (W/L)_1 (V_{GS} - V_T)^2 (1 + \lambda V_{DS1}) \tag{3}$$

$$I_0 = \frac{1}{2} K'_n (W/L)_2 (V_{GS} - V_T)^2 (1 + \lambda V_{DS2}) \tag{4}$$

where K'_n is the process parameter given by, $K'_n = \mu C_{ox} \frac{W}{L}$. μ is the electron mobility (hole mobility) in NMOS (PMOS) devices, C_{ox} is the capacitance per unit area, $\frac{W}{L}$ is the aspect ratio of the MOS device with W as the gate width and L as the gate length, V_{GS} is gate to source voltage of the MOS transistor, V_{DS} is drain to source voltage of the MOS transistor and λ is the channel length modulation parameter. If we neglect the effect of channel length modulation, the ratio of the drain currents is given by

$$\frac{I_0}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \tag{5}$$

The currents I_0 and I_{REF} can be made equal if the width to length ratio of the two MOS devices are made equal.

2.3. Cascode current mirror

While designing simple current mirror, the effect of channel length modulation was neglected. This leads to significant error in copying currents. Thus instead of simple current mirrors, we can use cascode current mirrors in which the effect of channel length modulation is negligible. Fig. 2 shows the cascode current mirror circuit. The actual ratio of drain currents are given by

$$\frac{I_0}{I_{REF}} = \frac{(W/L)_4}{(W/L)_1} \frac{(1 + \lambda V_{DS4})}{(1 + \lambda V_{DS1})} \tag{6}$$

The output resistance of the cascode current source is substantially larger than that of the basic two-transistor circuit. Thus the load current in the cascode circuit is more stable against variations in output voltage [6,7].

3. Analog implementation of FFT

In DIT algorithm, the outputs are in the ascending order, whereas the inputs are in the bit reversed order, or in other words they are decimated. In analog FFT, symbols are denoted as currents using differential signalling. The representation of a complex signal needs four wires: two for real part and two for the imaginary part. For example, a complex signal $x[0]$ is represented using differential signalling, as given below
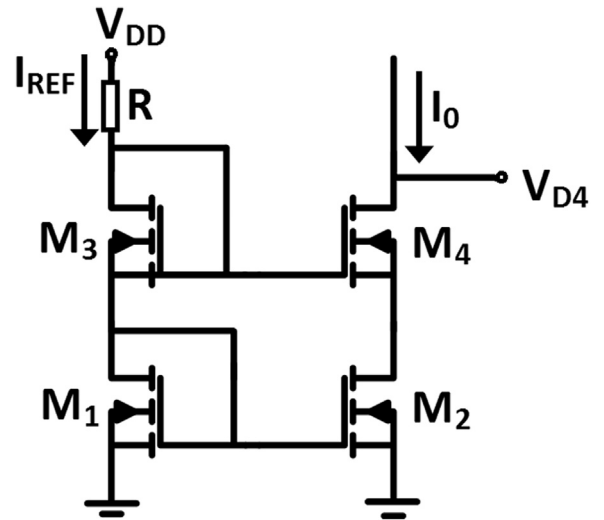

Fig. 1. Current mirror.

Fig. 2. Cacode current mirror.