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A 19.38 dBm OIP3 gm-boosted up-conversion CMOS mixer for 5–6 GHz application

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ABSTRACT

A highly linear up-conversion mixer for 5–6 GHz wireless local area network (WLAN) applications implemented using TSMC 0.18-μm standard complementary metal oxide semiconductor (CMOS) technology is presented. The feature of the proposed mixer is based on the double-balanced Gilbert cell with current-reused technique to enhance the third-order input intercept point (IIP3). Moreover, local oscillator (LO) body grounded and gm-boosting techniques are also integrated to boost the power conversion gain (CG). The proposed up-conversion mixer demonstrates a maximum CG of 7.21 dB, a maximum IIP3 of 13.17 dBm, an output third-order input intercept point (OIP3) of 19.38 dBm, and a DC power consumption of 4 mW on silicon given a 1.1 V supply voltage. The overall chip area including radio frequency (RF) pads is 1×0.85 mm^2, where the active area is merely 0.7×0.37 mm^2.

1. Introduction

The wireless multimedia services have become part of our daily lives, and in this respect, IEEE 802.11a/b/g/n wireless local area network (WLAN) standards are indispensable [1,2]. However, to keep pace with the rapid development of the information technology (IT), new communication systems/devices, such as smart phones, pads, cameras and even TVs, demand more reliable wireless links as well as higher data rate. Consequently, there is a requirement of coping capability for devices and standards with next-generation wireless communication systems [3]. Federal Communications Commission (FCC) announced a new protocol of IEEE 802.11ac WLAN standard for higher data rate of wireless communication systems. That is, if the data rate higher than 1000 Mbps, 160 MHz channel bandwidth from 5 GHz to 6 GHz is the one to be utilized [4].

To meet such high data rates, a highly linear mixer should be included in next-generation wireless communication systems, since the linearity has significant impact on the total linearity of a radio frequency (RF) front-end. Therefore, it is worthwhile investigating superior techniques for highly linear mixers. In general, third-order input intercept point (IIP3) and output intercept point (OIP3) are two important features to demonstrate the linearity of the CMOS RF front-end. Several techniques have been reported to enhance the IIP3 of RF mixer [5–12], which are all very sensitive to gate bias variations. Multiple gated transistors (MGTR) technique had been implemented by adopting two MOSFETs, where the overdrive voltage of each transistor is chosen to compensate for the nonlinear characteristics of the main transistor [5,6]. Derivative superposition (DS) using a negative gm in saturated pseudo-differential transistor (PDT) is compensated by the positive value of PDT in subthreshold region [7,8]. Passive mixers without consuming power consumption can achieve high linearity, since the level of undesired intermodulation products of these mixers is weaker than their active counterparts. However, they are suffered from conversion loss, poor isolation, and may require more amplifiers in upstream stages [9,10]. The third-order intermodulation distortion (IMD3) cancellation method realized that a common-source amplifier generates IMD3 signals with 180 phase difference against the IMD3 of the cascode main amplifier IMD canceller [11], and utilized negative impedances to simultaneously cancel flicker noise and IM3 in Gilbert-type mixers [12]. To eliminate the derivative nonlinearity, the previous studies utilized auxiliary transistors or circuits to drive the derivative coefficient close to zero. Although linearity could be improved through these approaches, extra transistors or circuit pay the price of high design complexity and more power dissipation. Furthermore, not only the linearity, but power conversion gain (CG) should also be taken into account with CMOS active mixers to alleviate the design margin of the following stages.

In this work, a wideband up-conversion mixer with high linearity and moderate power CG has been proposed, where gm-boosting, current-reused features are integrated. A prototype implemented using 0.18-μm CMOS process is demonstrated to meet the requirements of IEEE 802.11ac WLAN standard.

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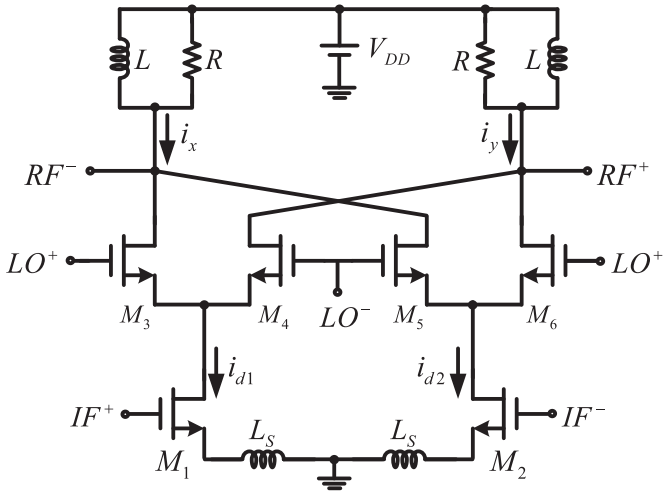

Fig. 1. Schematic diagram of the conventional up-conversion mixer [13].

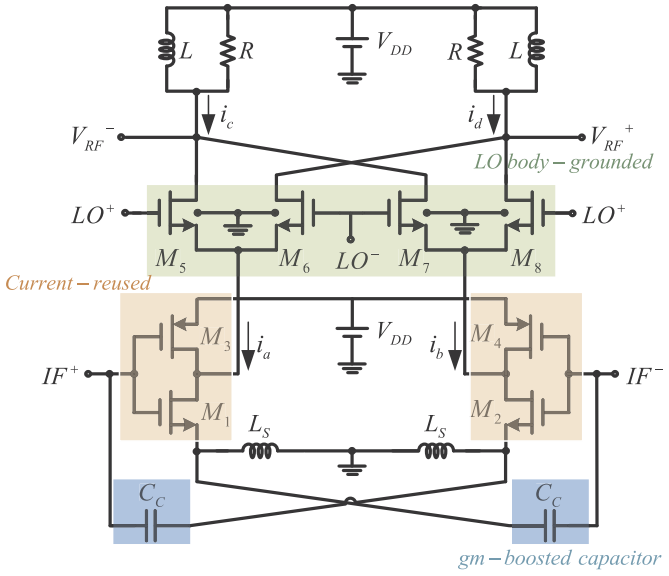

Fig. 2. Schematic diagram of the proposed up-conversion mixer.

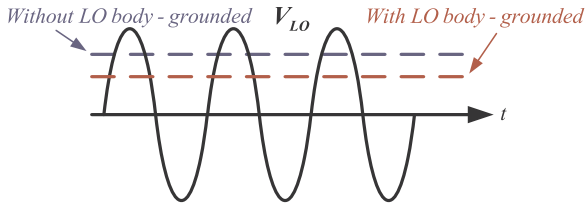

Fig. 3. Signal waveform diagram of the conventional CMOS switch.

2. Up-conversion mixer with high linearity

Many recent up-conversion mixers use the conventional double-balanced Gilbert-cell up-conversion mixer architecture [13] as shown in Fig. 1. The differential pair M_1–M_2 with degenerative inductance acts an IF transconductance stage. M_3–M_6 consist of the LO switching pair. Two modified output loads for high frequency are used to flatten the CG. The differential IF currents shown in Fig. 1, namely i_{d1} and i_{d2} in the S-domain, are expressed as follows:

$$i_{d1}(S) = -i_{d2}(S) = \frac{V_{IF}(S)}{2} \frac{g_{m1,2}}{1 + g_{m1,2} S L_S} \tag{1}$$

where g_{m1} and g_{m2} are the transconductance of NMOS transistor pair M_1 and M_2, respectively, S is equal to $j\omega$, and $V_{IF}(S)$ is the input signal, namely $V_{IF}\cos(j\omega_{IF}t)$. The differential output current of the conventional up-conversion mixer in time-domain can be attained by the following equation:

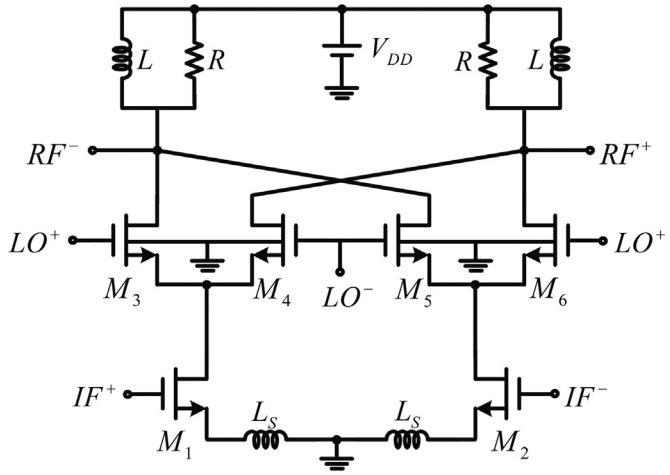

Fig. 4. Schematic of the conventional up-conversion mixer with LO body-grounded structure.

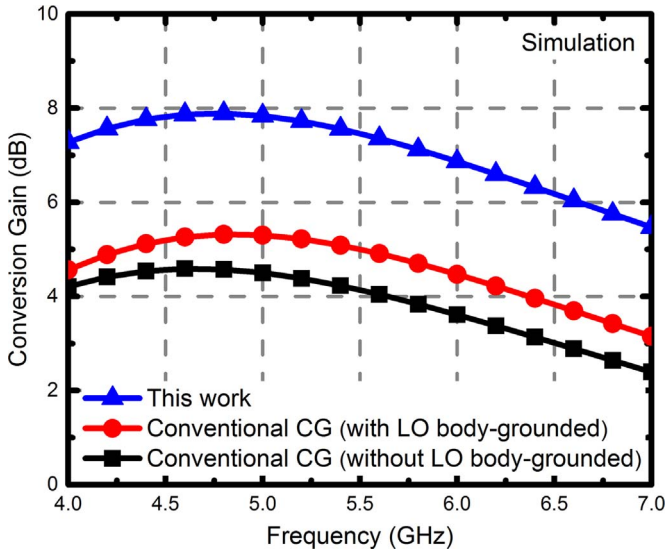

Fig. 5. Simulated CG comparison with conventional up-conversion mixer.

Table 1
Main parameters for conventional up-conversion mixer.

Mixer types	W/L (μm) (M_1/M_2)	W/L (μm) (M_3–M_6)	R (Ω)	L (nH)	L_S (nH)	V_{DD} (V)
Conventional Conventional (with LO body-grounded)	90/0.18	20/0.18	500	10	0.57	1.2

Table 2
Main parameters for the proposed up-conversion mixer.

Mixer types	W/L (μm) (M_1/M_2)	W/L (μm) (M_3–M_4)	W/L (μm) (M_5–M_8)	R (Ω)	L (nH)	L_S (nH)	V_{DD} (V)
This work	90/0.18	120/0.18	20/0.18	500	10	0.57	1.2