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Optimized thermal sensor allocation for field-programmable gate array temperature measurements based on self-heating test

Jingwei Li, Shiwei Feng*, Yamin Zhang, Chao Wang, Xin He

College of Electronic Information & Control Engineering, Beijing University of Technology, Beijing 100124, China

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ABSTRACT

In this paper, an optimization method for ring oscillator (RO)-based thermal sensor allocation based on a fuzzy clustering algorithm is proposed. A sensor array is distributed uniformly on a field programmable gate array (FPGA) as an original layout. Using a trade-off between sensor numbers and measurement resolution, the thermal sensors are combined based on their mutual clustering levels, which are inversely proportional to the temperature difference. This method is suitable for various applications on FPGAs. A self-heating test module that uses the FPGA resources to generate hotspots and large temperature gradients for measurement validation is presented. The experimental results show that when the temperature gradients range from 0 °C up to 40 °C on an Altera Cyclone IV FPGA, we can reduce sensor resource requirements by 37.5% while maintaining a measurement resolution of 1 °C.

1. Introduction

With their large-scale programmable logic resources and variety of integrated intellectual property (IP) cores, field-programmable gate arrays (FPGAs) are widely applied in complex digital systems. To satisfy their performance, cost and power requirements, FPGAs are currently developed using the most advanced nanoscale semiconductor processes available [1,2]. However, the successive process shrinkages that have driven the increased integration and capabilities of semiconductor devices have also presented the critical problems of increasing leakage power, higher peak temperatures, and degraded performance levels [1,3,4], that make thermal awareness of FPGAs increasingly important in both the manufacturing and in-field operation phases to ensure device reliability [5].

Increasing numbers of thermal management techniques are provided in FPGA-based thermal testing to avoid large thermal gradients. Accurate temperature measurement and prediction can improve the thermally aware test scheduling performance of these devices, especially for chips with multiple cores [6]. Ring oscillators (ROs) are widely used as thermal sensors on FPGAs and can measure the transient in-field chip temperature [7–12]. Many researchers dynamically insert, operate, and eliminate RO-based sensors using reconfigurable technology [10,13]. This method can save hardware resources and reduce the effects of these sensors on temperature during the test procedure. However, high-speed reconfigurable technology is only supported by a few advanced FPGAs, and it is difficult to control in terms of task migration and test scheduling during thermal management testing. Another approach is to integrate the ROs with the test circuit and operate them synchronously at runtime. Static placement of the devices, however, occupies significant quantities of resources, power consumption and incurs a communication overhead to read back measured values from the sensors, and thus represents a significant challenge for thermal sensor design and placement. In this paper, we propose a novel method for optimized thermal sensor allocation based on a fuzzy clustering algorithm. The sensors are clustered based on the temperature distribution. Using the results of the optimization method, we can obtain more temperature distribution information while using fewer sensors. To simulate the actual experimental conditions, we configure a self-heating test module using the rich programmable logic resources on the FPGA, which can provide both hotspots and large temperature gradients at runtime. We also compared optimization results corresponding to different gradients on several chips to validate the proposed method.

The rest of the paper is organized as follows: Section 2 gives an overview on the related work. We discuss our optimization methodology and self-heating test module in detail in Section 3. Experiment results with detailed implementation process and comparison of the results of the method application are reported in Section 4. Finally we conclude the paper in Section 5.

* Corresponding author.
E-mail address: shwfeng@bjut.edu.cn (S. Feng).

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2. Related work

RO-based thermal sensors can be implemented using small numbers of digital logic resources at arbitrary locations on FPGAs, which thus increases both the applicability and the flexibility of these sensors. Related works involving FPGA-based thermal sensors have either suggested a regular rectangular grid, or an irregular arrangement focused on expected application-specific hotspots [11]. For example, Zick and Hayes [7] placed more than 100 RO-based sensor nodes on a Xilinx Virtex-5 FPGA for online measurement of its thermal parameters. They recommend a hexagonal tessellation grid as their spatial arrangement of sensors due to its efficient area coverage. Lopez-Buedo et al. [10] inserted temporary arrays of sensors in the free space on the FPGA when required, relying on dynamic reconfiguration at runtime.

Most work on FPGAs involves between 1 and 32 sensors per chip [7]. Ideally, the sensor density should be high enough to match the finest spatial granularity of the physical phenomena being sensed. Higher sensor densities can enable increased accuracy, for instance, in predicting chip lifetimes [12].

In our previous work [9], we proposed a thermal sensing network composed of 24 ring oscillators. The sensors used a completely logic cell-based design that can measure the transient thermal characteristics of the die. We also compared our temperature distribution results with those measured using infrared thermal imagers for accuracy verification.

Ruething et al. [14] proposed a methodology for sensor performance evaluation, and studied the effects of different RO design spaces on sensor noise, resolution and performance. Recently, Weber et al. [15] conducted research on sensor calibration for FPGA thermal measurements. However,

Mukherjee et al. [13] allocated the sensors using a recursive bisection method for a given distribution of hotspots within a predefined error margin to effectively minimize the number of sensors and determine their placement throughout the fabric of the FPGA, the average number of sensors they used is found to be 19.11 compared with that for Grid-based placement is 80.8. However, the measurement accuracy and variation of the thermal gradients in the temporal domain are not mentioned.

In this paper, we propose a method to optimize the uniform distributed sensor network layout for accurately capturing the on-chip thermal map with a minimum number of temperature sensors. We cluster the sensors using fuzzy clustering algorithms in terms of the actual temperature distribution to balance and simplify our sensor network. Unlike [13], our work analyzed temperature in both temporal and spatial domains for widely different application, and the optimized allocation is a result of a trade-off between the number of sensors and the measurement resolution. Similar to other works in this field [5,16], we present a self-heating test module to heat up the FPGA and provide hot-spots and large thermal gradients. The temperature variation is measured in the temporal and spatial domains by the sensors.

3. Methodology

In this section, we introduce our approach for reasonable allocation of the thermal sensors, which is a result of iterative sensors clustering. A sensor array is distributed uniformly on FPGA as an original layout. We study the temperature characteristics measured by the sensor array using the fuzzy clustering method to determine their similarities. Therefore, we can determine the sensors that should be withdrawn based on their approximation degree. The detail sensors clustering method is described as follows. We also demonstrate the self-heating test module used to generate heat on the FPGA to simulate the practical application for experimental validation.

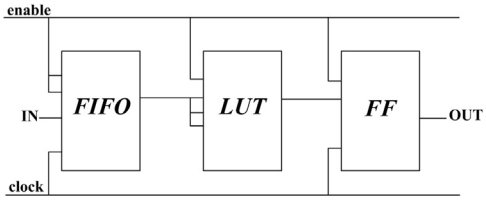

Fig. 1. Schematic of self-heating element.

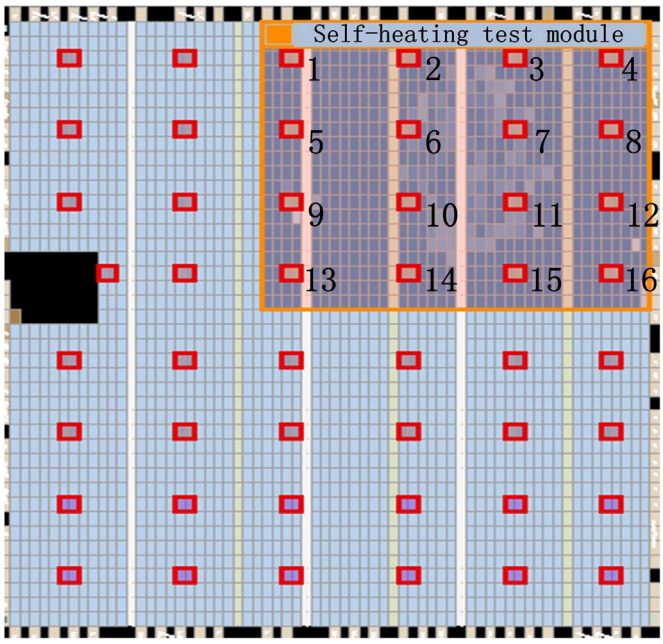

Fig. 2. Floor map of the FPGA.

3.1. Self-heating test module

To increase the chip temperature, we simulate heat sources using the configurable logic resources on the FPGA. A single self-heating element is composed of a first-in first-out (FIFO) block, a LUT and a flip-flop (FF), as shown in Fig. 1.

A turning input signal is written by the FIFO and read out with the clock operation, and then the data is output through a four-input LUT and a clock-controlled FF. The input signal is connected to a clock for heating of the FPGA to the greatest extent. The self-heating element is controlled using an enable signal. Multiple self-heating elements constitute the heat sources arranged in series. In this way, the heat is generated by the continuously turning signal and clock triggering, and the actual temperature gradient distribution result is measured using the RO-based sensors.

3.2. Sensor clustering

To reduce the number of sensors required and also reduce the effects of the temperature information as far as possible, we study the temporal and spatial temperature characteristics to determine the similarities of sensor points for resource reorganization. Based on the fuzzy clustering method, we quantify the relation between sensor network's resolution and sensors allocation. The optimum allocation maybe derived from multiple iterative calculations in particular resolution requirements, and the method for once iteration includes the following steps:

a.: Establish a domain $U = \{x_1, x_2, \ldots, x_n\}$ in which the thermal sensors are to be classified, where every object has m indicators for its characteristics, i.e., $x_i=\{x_{i1}, x_{i2}, \ldots, x_{im}\} (i = 1,2,\ldots,n)$. Taking the temperature into account as the critical characteristic, we collect the temperatures measured by the sensors at 1 min intervals at run time,