



A low energy ASIC for triple-chamber cardiac pacemakers with contact resistance measurement



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ABSTRACT

A mixed-signal application specific integrated circuit (ASIC) is presented for triple-chamber pacemakers. To save power, a programmable stimulator composed of a 5-bit low-voltage digital-to-analog converter (DAC) and a triple-mode voltage multiplier is introduced to lower the capacitive load of the charge pump, thus reduces the charge pump driving clock frequency to 100 Hz leading to significant reduction in dynamic power. According to refractory periods of the heart, a low-power control strategy is adopted in the sensing channel, in which the opamp is turned on by a sensing command and turned off automatically by a valid sensing event to reduce the average power consumption. Contact resistance measurement function based on bidirectional current injection is also integrated in the ASIC to reflect the connection status and pathological status of the patient's heart. The ASIC is fabricated in a 0.35- μm Bipolar-CMOS-DMOS (BCD) process with a chip area of $3.8\text{ mm} \times 3.8\text{ mm}$. Measurement results show that the magnitude of the stimulus pulse can be programmed from 0.1 to 7.5 V with 0.1-V step. Almost linear heart resistance measuring is achieved in the resistance range of 250–4000 Ω . The average current consumption is 4 μA under typical pacing algorithms from a 2.8-V power supply.

1. Introduction

Modern artificial cardiac pacemakers are very sophisticated implantable medical devices used to maintain an adequate heart rate when the natural pacemaker is not fast enough [1]. The complex operations of pacemakers are realized both by intelligent treatment algorithms and elaborately designed function circuits to execute the algorithms. As implantable medical devices, small size and low power consumption are primary requirements for cardiac pacemakers. Normally, the treatment algorithms are implemented in software method by ultra-low power microprocessors whose performances are improved greatly with the advances in IC technologies. Whereas, most of the function circuits (such as sensing circuits, stimulating circuits and etc.) are analog and their performances and power reduction are not benefited so much from the advances in IC technologies. Thus, due to the rigorous limitations of size and power consumption in pacemakers, the function circuits need to be carefully designed to achieve high integration and low power as far as possible, especially for triple-chamber pacemakers. Hence, for this motivation, this work aims at implementing a low-energy application specific integrated circuit (ASIC) which contains most of the necessary function circuits for

triple-chamber pacemakers.

Single chamber pacemakers are capable of sensing and stimulating only one chamber of the heart. However, it was found that in some patients there were obstacles during the excitation transferred between atria and ventricle (i.e. AV block) [2]. In these cases, dual chamber pacemakers are more appropriate by sensing both the atria and the ventricle and stimulating one or both of them. However, for some patients suffering from heart failure, their left and right ventricles do not beat in unison [3] and dual-chamber pacemakers are unable to deal with this situation. Therefore, triple-chamber pacemakers have been developed to carry out cardiac resynchronization therapy (CRT) for patients with severe heart diseases which couldn't be treated by dual-chamber pacemakers [1]. Compared with dual-chamber counterparts, left ventricle stimulation is added in triple-chamber pacemakers to synchronize the beating of the two ventricles. As more functions are required to manage the rhythms of the three chambers in the heart, the low power consumption becomes critical in order to extend the battery life. Furthermore, additional number of leads in triple-chamber pacemakers increases the chances of loosening or detachment of electrode leads due to frictions or movements of human body, which could lead to malfunction of implanted pacemakers. An effective method to detect

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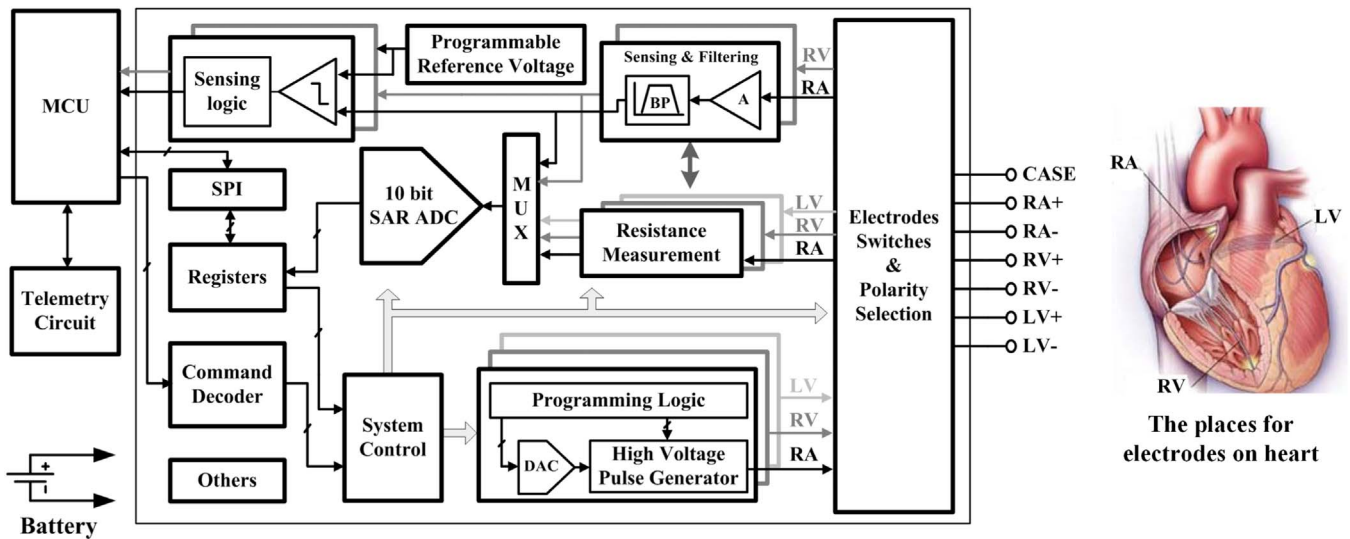


Fig. 1. System diagram of the proposed triple-chamber pacemaker.

the status of electrode connection is to perform contact resistance measurement. The measurement results of contact resistance can also be used to reflect pathological status of the patient's heart [4].

Triple-chamber cardiac pacemakers are commercially available from several companies. However, as noted in [5], because of the "closed" characteristic of pacemaker industry, only a little information is published in the open literature regarding the circuit design of cardiac pacemakers and even less for ASICs. Among the limited open literatures in the area of ASIC design for pacemakers, most reports are focused on the sensing functions (acquiring and processing of the heart beating signals) [6,7], several are about the circuit design regarding the pacing function [8–10]. Only a few reported ASICs implement the full functions of a pacemaker including both sensing and pacing. However, these works are either for single-chamber [11] or for dual-chamber pacemakers [12]. Moreover, the contact resistance measurement function was seldom reported in prior arts.

Power consumption is of great importance for implantable pacemakers. Powered by a lithium-ion based battery about 1-Ah capacity, the total average current dissipation is required to be less than 11 μ A to achieve an over 10-year life time [5], which is an extremely challenge for triple-chamber pacemakers. Among all the functional blocks, the high-voltage pulse generator for pacing in a pacemaker consumes most of the power. For example, the high-voltage stimulator along with charge pump and pulse generator in [11] consumes up to 25.5 μ W (10 μ W for charge pump and 15.5 μ W for pulse generator respectively), while the monitoring analog front-end consisting of preamplifier, filter and 8-bit ADC only consumes 236-nW. This is because the charge pump is directly connected to the large pacing capacitor requesting large driving capacity and high clock frequency, which consumes large power [9,11]. Thus, to achieve an over 10-year life time for a triple-chamber pacemaker, power efficiency must be improved for the pacing circuits.

In the sensing channel, the low-frequency in heart beating signals together with possible large interferences pose challenges in the design of the front-end amplifier and filter. Capacitive feedback [13,14] and g_m -C [15] architectures were adopted for the front-end filters to avoid external passive components. However, the gain and/or filter bandwidth of these topologies are still prone to variations in technology and supply voltage. Auxiliary circuit blocks for calibrations may lead to large chip area and power consumption. On the other hand, the classical active-RC topology with several external components has advantages of low power, and accurate gain and bandwidth over large variations in technology and supply voltage [5].

In this paper, a low power mixed-signal ASIC for triple-chamber

cardiac pacemakers aimed at CRT applications is presented (first reported in [16]). To improve the efficiency of the pacing circuits, a programmable stimulator composed of a 5-bit low-voltage DAC and a triple-mode voltage multiplier is proposed to reduce the capacitive load of the charge pump, where the clock frequency of the charge pump is lowered to 100 Hz leading to tens of times reduction in dynamic power compared to existing designs. In the sensing channel, a fully differential active-RC topology with several external passive components is adopted for the front-end amplifier to ensure accurate gain and bandwidth. Furthermore, a low-power systematic control strategy is employed to reduce the average power consumption by turning off the op-amp when the sensing function is not required. Contact resistance measurement function based on bidirectional current injection is also integrated in the ASIC to determine the connection status of the leads and electrodes and pathological status of the patient's heart.

The rest of the paper is organized as follows. Section 2 presents the ASIC system architecture. In Section 3, the programmable stimulator and the proposed high-voltage multiplier, programmable logic, high-efficiency charge pump are explained in detail. Sections 4 and 5 report the implementation of the sensing channel and the resistance measurement, respectively. The measurement results are presented in Section 6. Section 7 draws the conclusion.

2. System architecture

The system diagram of the proposed triple-chamber pacemaker system is presented in Fig. 1. Normally, all the circuits are packaged in a titanium case and implanted under the skin of the chest. Different from single or dual chamber pacemaker, the triple-chamber pacemaker has 3 pairs of leads connected to 3 pair of electrodes installed in the right atrium (RA + /RA –), right ventricle (RV + /RV –) and left ventricle (LV + /LV –), respectively. With the CASE terminal, which is connected to the case of pacemaker, each pair of electrodes can be configured into either unipolar or bipolar mode [5].

As the core of the pacemaker system, the proposed ASIC performs three major tasks: 1) acquiring and processing the heart beating signals from RA and RV to estimate the magnitude and rate of the heart beating signals. To ensure flexibility, heart beating signals from any 2 of the 3 chambers can be measured by changing the configuration of the switch network, and RA and RV are measured by default. 2) Measuring the contact resistance of three chambers independently to diagnose the attachment status of the electrodes and provide additional information about the pathological status of the patient's heart; 3) Generating stimulus pulses to each chamber with programmable magnitude and

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