# A scalable decimation filter ASIC for high resolution digital magnetometer with sigma-delta modulator feedback loop

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## ARTICLE INFO

## ABSTRACT

High-resolution digital magnetometers often use sigma-delta modulator feedback loops for large dynamic range, good linearity and low power consumption. A decimation filter is usually needed to obtain the high-resolution output data and reduce the output data rate at the same time. A scalable decimation filter application specific integrated circuit (ASIC) for high-resolution digital magnetometer with sigma-delta modulator feedback loop has been designed, implemented and fabricated. Keeping the decimation ratio of 128 to 1 fixed, the ASIC chip was carefully designed to be scaled with input data rate accordingly, thus maintaining the same resolution of 24 bits for the digital magnetometer. The ASIC chip consists of a cascaded integrator-comb (CIC) filter decimated by 16, a droop compensation programmable FIR1 filter decimated by 4, a brick-wall programmable FIR2 filter decimated by 2 and a 5th order sigma-delta bit stream generator for built-in-self-testing (BIST). The chip was designed and fabricated based on the GlobalFoundries 0.18 μm CMOS process. Its total die size is about $3 \times 3$ mm$^2$, having 256,000 equivalent logic gates. In a typical working scenario with an input data rate of 128 kHz, the measured power consumption of the core powered with 1.8 V is about 0.9 mW.

## 1. Introduction

Fluxgate magnetometers have been widely used for all kinds of magnetic field investigations in space such as accurate earth magnetic field measurements, planetary magnetism, interplanetary magnetic fields and solar wind interactions with celestial bodies [1,4]. Both the traditional analogue and the more recently developed digital readout electronics for fluxgate magnetometers use high-resolution analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) chips for signal quantization. The disadvantages of such converter components are the high power consumption, large mass and poor linearity over the interested dynamic range [2].

Driven by these considerations, a new electronic design for fluxgate magnetometer readout was proposed that uses a sigma-delta modulator control loop. This kind of magnetometer design provides direct digital output without the use of a separate analogue-to-digital converter chip [3–7], but it needs a field-programmable gate array (FPGA) or a digital signal processor to remove the quantization noise and obtain high resolution data [4]. J. Piil-Henriksen [5] described such a fluxgate magnetometer, based entirely on digital signal processing and digital feedback control, thereby replacing the classical second harmonic

tuned analogue electronics by processor algorithms. Erik B. Pedersen [6] proposed a fluxgate magnetometer for Astrid-2 satellite using mathematical routines, implemented by software for commercially available digital signal processors, to determine the magnetic field from the fluxgate sensor. W. Magnes [7] developed an instrument front-end ASIC (0.35 μm CMOS from Austria microsystems) for magnetic field sensors based on the fluxgate principle. It is based on a combination of the conventional analogue readout electronics of a fluxgate magnetometer and a sigma-delta modulator control loop for direct digitization of the magnetic field. The analogue part is based on a modified 2-2 cascaded sigma-delta modulator. The chip area is 20 mm$^2$ and the total power consumption is about 60 mW. It has been demonstrated that the overall functionality and performance of the magnetometer front-end ASIC is sufficient for scientific applications in space.

## 2. Asic chip architecture

Digital fluxgate magnetometers with a sigma-delta modulator control loop for a direct digitization of the magnetic field usually employ a modified 2-2 cascaded sigma-delta modulator due to the good
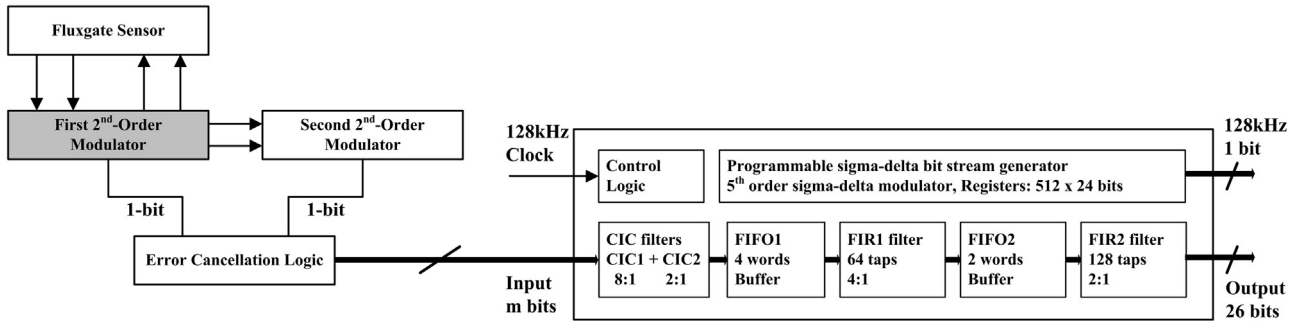
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**Fig. 1.** Digital fluxgate magnetometer with the decimation ASIC chip architecture.

stability of the second-order modulator. Error cancellation logic is used to combine the two second-order modulator outputs. The resultant m-bits data from the error cancellation logic will have noise shaping properties of the fourth-order sigma-delta modulator. The task of the decimation filter ASIC is to extract the useful low frequency signals. The whole ASIC chip consists of a CIC filter, a first in first out (FIFO) FIFO1, a finite impulse response (FIR) FIR1 filter, a FIFO2, a FIR2 filter, a control logic module and a sigma-delta bit stream generator, as shown in Fig. 1.

The CIC filter is a class of hardware-efficient linear phase finite impulse response digital filters. CIC filters achieve sampling rate decrease (decimation) without using multipliers, so they are widely deployed as the first stage of decimation filters [8–10]. Our CIC filter was designed with two cascaded sections, CIC1 and CIC2. CIC1 is a single stage 5th order fixed decimation by 8 CIC filter, and CIC2 is a single stage 6th order fixed decimation by 2 CIC filter. A FIFO buffer FIFO1 is used to bridge the CIC filter and FIR1 filter. It has 4 words in depth, buffering input data from CIC filter. The FIR1 filter stage has a decimation by four FIR filter structure. It compensates for the CIC filter droop and flattens the magnitude response of the pass band. It can store 60-taps 24-bits wide programmable coefficients. Another FIFO buffer FIFO2 is used to bridge the FIR1 filter and FIR2 filter. It has 2 words in depth, buffering input data from FIR1 filter. The FIR2 filter stage has a decimation by two FIR filter structure. It creates a low-pass brick wall filter to block all the aliased components from down-sampling. It can store 126-taps 24 bits wide programmable coefficients. The control logic module is used to generate logic signals to control, coordinate and synchronize the CIC filter, the FIFO1, the FIR1 filter, the FIFO2 and the FIR2 filter. The bit stream generator generates a built-in-self-testing (BIST) sigma-delta bit stream. It can be programmed to generate 5th order sigma-delta bit stream containing known signals for simulation, verification and measurement at different development stage of the decimation filter ASIC chip.

## 3. Design and implementation

### 3.1. CIC filter design and implementation

A CIC filter consists of an equal number of stages of ideal integrator filters and comb filters. The cascaded integrator-comb filters were first proposed by Eugene Hogenauer [8]. Its frequency response may be tuned by selecting the appropriate number of cascaded integrator and comb filter pairs. The highly symmetric structure of a CIC filter allows efficient implementation in hardware [9–14].

Our CIC filter was designed with two cascaded sections, CIC1 and CIC2. The first section is CIC1, a single stage 5th order fixed decimate by 8 CIC filter, having 36 coefficients. This CIC filter decimates the 128 kHz incoming m-bit sigma-delta bit stream from the modulators down to a 16 kHz data rate. Eq. (1) shows its transfer function and Fig. 2 shows its frequency response and the aliasing noise to the passband. The requirement for this CIC filter is that its aliasing noise to the passband is less than −130 dB when down-sampled by 8.
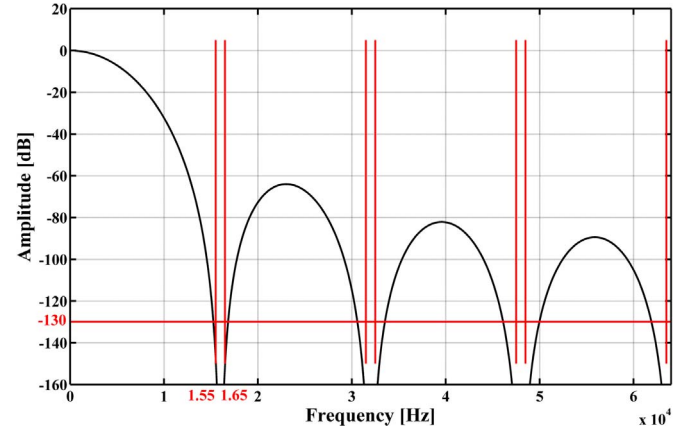


**Fig. 2.** Frequency response of the designed CIC1 filter.

$$H(z) = \left( \frac{1 - z^{-8}}{1 - z^{-1}} \right)^5 \tag{1}$$

A more economical realization of CIC1 filter is provided by the Hogenauer structure [9–11], as shown in Fig. 3. This structure is obtained by factoring the transfer function of CIC1 filter as follows.

$$H(z) = \left( \frac{1}{1 - z^{-1}} \right)\left( \frac{1}{1 - z^{-1}} \right)\left( \frac{1}{1 - z^{-1}} \right)\left( \frac{1}{1 - z^{-1}} \right)\left( \frac{1}{1 - z^{-1}} \right)\left( \frac{1 - z^{-8}}{8} \right)$$
$$\left( \frac{1 - z^{-8}}{8} \right)\left( \frac{1 - z^{-8}}{8} \right)\left( \frac{1 - z^{-8}}{8} \right)\left( \frac{1 - z^{-8}}{8} \right) \tag{2}$$

and realizing each factor by an accumulator or a differencing stage.

The second section is CIC2, a single stage 6th order fixed decimate by 2 CIC filter, having 7 coefficients. This CIC2 filter decimates the incoming data from CIC1 from a rate of 16 kHz down to 8 kHz. Eq. (3) shows its transfer function. Fig. 4 shows its frequency response and the aliasing noise to the passband. The requirement for this CIC filter is that its aliasing noise to the passband is less than −130 dB when down-sampled by 2.

$$H(z) = \left( \frac{1 - z^{-2}}{1 - z^{-1}} \right)^6 \tag{3}$$

The realization of CIC2 is the same as the above CIC1, as shown in Fig. 5, but having one more factor for the accumulator of the difference stage and down-sampling by 2.

### 3.2. FIFO design and implementation

Two FIFO buffers, FIFO1 and FIFO2, are used to bridge the CIC filter and FIR1 filter, and FIR1 filter and FIR2 filter in our design. FIFO1 has a 4×24 bits structure, buffering input data from CIC filter, and FIFO2 has a 2×24 bits structure, buffering data from FIR1 filter. For a period of 128 clock cycles, the CIC filter outputs (or writes) 4 words data to