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A high accuracy CMOS subthreshold voltage reference with offset cancellation and thermal compensation

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ABSTRACT

This paper presents a high accuracy CMOS subthreshold voltage reference without BJTs for the low-supply-voltage and low-power application. The low supply voltage and low power dissipation are achieved, by making MOSFETs work in the subthreshold region. Besides, the offset scaling down (OSD) technique is proposed for the first time to cancel out the reference voltage variation caused by the offset of the clamping OTA. In addition, the pseudo-series-diodes are used with the negative temperature coefficient (TC) impendence for the second-order thermal compensation. Finally, the proposed voltage reference circuit is implemented in a standard 0.13 μm CMOS process, while the active silicon area is about 0.15×0.24 mm^2. At the minimum supply voltage 0.6 V, the measured results shows a TC of 12.8 ppm/°C in the range of −25–85 °C, and total power consumption of 373 nW. The line regulation is 0.15 mV/V in the supply voltage range of 0.6–1.8 V, and the variation of the reference voltage (σ/μ) is 1.28% without trimming and 0.42% after trimming, respectively. The power supply rejection ratio (PSRR) without any filtering capacitor at 1000 Hz is −51 dB for 0.6 V supply and −73.8 dB for 1.8 V supply, respectively.

1. Introduction

The interaction between the medicine and microelectronics promotes the development of the diagnosis devices which are capable of monitoring healthy signs. These biomedical integrated circuit systems can be used on the surface of the skin or, even implanted into the body. For convenience, the implantable device must meet some important specifications, such as micro-size, high accuracy, low supply voltage (< 1 V), and ultra-low power consumption (< 0.5 μW) [1]. And in the implantable biomedical system, the voltage reference is a very important building block for generating a constant DC voltage independent of process, supply voltage and temperature variations, and attracts more and more interests. Although traditional BJTs-based voltage references can provide a fairly precise DC voltage with a small curvature temperature effect, it requires a high supply voltage because of the fixed 0.6–0.7 V p-n junction forward voltage [2,4]. Therefore, CMOS subthreshold voltage references without BJTs have received much attention since they can operate at low supply voltages and consume very low power [5,11].

The basic principle of the proposed voltage reference is based on the difference of gate source voltages (ΔV_{gs}) of NMOS transistors, which is so called as V_{TH}-based reference [6]. However, the precision of this reference often suffers from the variations over process, supply voltage or temperature (PVT). In order to generate the proper ΔV_{gs}, a clamping OTA is always needed in this kind of voltage reference circuit. However, the offset of this OTA will seriously affect the accuracy of the reference voltage [2,3]. Therefore, a chopper technology has been adopted to cancel out the offset of the OTA, making the deviation σ/μ of the reference output voltage less than 1.81% [4]. But the chopper technology needs an extra clock generation circuit and a low pass filter circuit, which increases the chip area and power consumption.

In addition, CMOS subthreshold voltage references always have poor TC [9], because the threshold voltage V_{TH} has larger second-order dependency over temperature than the V_{BE}. Therefore, for efficiently reducing the TC of the reference, the second-order thermal compensation is realized by using the MOSFETs in the deep triode region to replace the traditional resistors [9–11]. However, their supply voltage cannot be less than 1 V due to the limitation of the circuit structure, which is not suitable for the low voltage applications.

In order to improve the accuracy affected by the clamping OTA offset error and optimize the TC of the voltage reference, this paper presents a high precision, low TC, low power subthreshold CMOS

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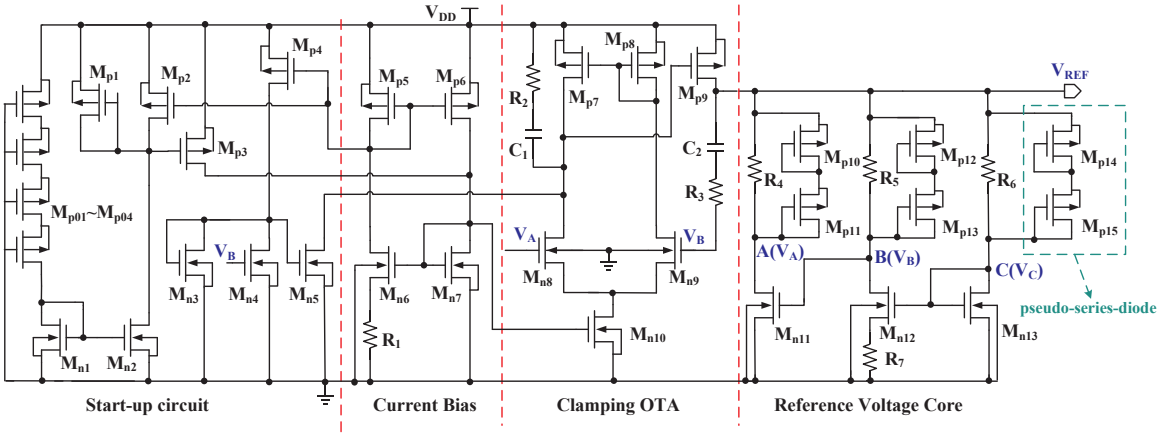

Fig. 1. Schematic of the proposed voltage reference.

voltage reference. For decreasing the OTA offset, an OSD technique is proposed for the first time, adopting the additional loop. And for lowering the TC of the voltage reference, the pseudo-series-diodes are used for the second-order thermal compensation, especially at a low supply voltage. Besides, to further improve the accuracy, a 3-bit trim network is added in this voltage reference.

This paper is organized as follows: Section II describes the operation principle of the proposed voltage reference and the circuit configuration in detail; the simulated and measured results are shown and compared with the other competitors in Section 3. Finally, the conclusion is given in Section 4.

2. The proposed voltage reference

This paper proposes a low voltage reference with high accuracy. Fig. 1 shows the detail of the proposed voltage reference circuit, which is composed of the reference voltage core, the clamping OTA, the start-up circuit and the bias circuit. All of the transistors are biased in subthreshold region except M_{p01}-M_{p04}. To generate nano-ampere start-up current, M_{p01}-M_{p04} works in deep triode region to replace the traditional resistors. M_{p3} and M_{n5} provide the start-up current for the bias circuit and reference voltage core respectively. M_{p5}, M_{p6}, M_{n6}, M_{n7} and R_1 constitute a bias circuit which works as a supply-voltage-independent current source for the clamping OTA. The clamping OTA is used for two purposes. Firstly, it makes the voltage at node A and B equal. Secondly, it improves the PSRR performance at the low supply voltage. C_1, C_2, R_2 and R_3 can compensate the whole loop to ensure the stability. Because M_{n11}~M_{n13} all work in the subthreshold region, their current can be expressed as Eq. (1) [6].

$$I = \mu \frac{W}{L} C_{ox} V_t^2 e^{\frac{V_{gs}-V_{TH}}{\eta V_t}} \left(1 - e^{-\frac{V_{ds}}{V_t}}\right) \tag{1}$$

Where $V_t = kT/q$ is the thermal voltage (k is the Boltzmann constant, q is the elementary charge and T is the absolute temperature), V_{TH} is the threshold voltage of a MOSFET, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, and η is the subthreshold slope factor. V_{gs} and V_{ds} are the gate-source and drain-source voltages respectively. When V_{ds} is larger than several V_t, the current I in Eq. (1) can be approximated by Eq. (2), and so the gate-source voltage V_{gs} can be expressed as Eq. (3).

$$I = \mu \frac{W}{L} C_{ox} V_t^2 e^{\frac{V_{gs}-V_{TH}}{\eta V_t}} \tag{2}$$

$$V_{gs} = \eta V_t \ln \frac{I}{\mu \frac{W}{L} C_{ox} V_t^2} + V_{TH} \tag{3}$$

M_{p10} and M_{p11} constitute a pseudo-series-diode, which can be considered as a resistor R_p, and whose resistance is dependent on the voltage V_{gs} and V_{TH}. Similarly, M_{p12}, M_{p13} and M_{p14}, M_{p15} also constitute two pseudo-series-diodes, which also have the same equivalent resistance of R_p. As mentioned above, the clamping OTA can make the voltage at node A equal to that at node B, which means $V_A = V_B$. Therefore, M_{n11} can be regarded as a diode-connected transistor same with the transistor M_{n13}. Besides, the resistors R_4, R_5 and R_6 have the same resistance, and the size ratio of M_{n11},M_{n12},M_{n13} is 1:n:1. Since the symmetry of M_{n11} and M_{n13}, it can be approximately considered that $V_A = V_C$. Based on the above derivation, it can be understood that $V_A = V_B = V_C$. Therefore, the voltage across R_7 is equal to the difference between V_{gsMn13} and V_{gsMn12}, which can be expressed as (4), while the reference voltage V_{REF} can be expressed as (5).

$$\Delta V_{gs} = V_{gsMn13} - V_{gsMn12} = \eta V_t \ln n \tag{4}$$

$$V_{REF} = V_{gsMn11} + I_{PTAT}(R_p \| R_5) = V_{gsMn11} + \frac{R_p \| R_5}{R_7} \eta V_t \ln n \tag{5}$$

where the thermal voltage V_t increases linearly with temperature, but V_{gsMn11} changes with temperature as a high order term, which makes the TC of V_{REF} deteriorate. In addition, the OTA offset also influences $\eta V_t \ln n$ [2–4], which will cause serious variation of V_{REF}. For solving these two problems, the techniques of offset cancelling and thermal compensation have been adopted in the proposed voltage reference. Detail about these two solutions are presented as follows.

2.1. Cancelling out the offset voltage

In order to reduce the influence of the clamping OTA offset, this paper proposes an OSD structure, as shown in Fig. 2. For easy understanding, in Fig. 2, the equivalent resistors R_4', R_5' and R_6' represent the resistors in parallel with the pseudo-series-diodes in Fig. 1. The resistor R_7 represents the 3-bit trim network which calibrates the reference voltage.

Compared with the traditional clamping circuits, an additional branch of the resistor R_4' and the transistor M_{n11} is added, so that the clamping OTA clamps V_A and V_B rather than V_B and V_C. However, due to the OTA offset voltage, the voltage V_A and V_B are unequal actually. This offset voltage $|V_{OS}|$ can be expressed as Eq. (6).

$$|V_{OS}| = |(V_A + \Delta V_A) - (V_B + \Delta V_B)| = |\Delta V_A - \Delta V_B| \tag{6}$$

where ΔV_A and ΔV_B represent the variation of V_A and V_B caused by the OTA offset, respectively.

Assuming $R_4' = R_5' = R_6' = R'$, and with the reference voltage variation denoted by ΔV_{REF}, the variation of V_C ban be expressed as ΔV_C in Eq. (7), where $1/g_{mn13}$ is the small signal impedance of the transistor M_{n13} from the source to the drain.