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# Triple transistor based fault tolerance for resource constrained applications

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ABSTRACT

Fault tolerance has become essential for safety-critical applications like avionics, space, defense, automotive, bio-medical etc., where redundancy must be added to increase the systems' reliability. Incorporation of fault tolerance costs for extra hardware, time and power overhead that limits the use of existing fault tolerant methods in resource constrained applications like satellite, aircraft, surgical equipment, railway, motor vehicles etc. In this paper, we propose a new fault tolerant triple transistor (TT) method, which requires much lesser area overhead compared to the existing methods making it suitable in providing good reliable solutions for various resource constrained applications. In the TT method, redundancy has been added at the transistor level assuring good fault coverage. Theoretical as well as extensive simulation results have been provided to compare our new method with the existing ones and to highlight the advantages and disadvantages of the same.

## 1. Introduction

Adding redundancy at transistor level is beneficial in providing built-in immunity to the defects within a circuit and offers higher fault coverage compared to when the redundancy is added at higher level of abstraction [1]. Importance of fault tolerance has been increased in recent time due to the increase in probability of failures of chips because of the high integration ratio of the transistors. Hardware fault tolerant methods can be broadly categorized as static and dynamic. Dynamic reconfiguration method [2] is efficient in terms of area and power consumption compared to the static methods because of selected activation of spare modules only upon locating faulty active modules in the system; but static methods are capable of tolerating all sort of permanent, intermittent and transient defects and hence provides more robust solutions than dynamic methods [3,4]. Single event upsets (SEU) [5] are very common in satellite communications and space applications [6], whereas intermittent defects have become frequent in today's microcomputer systems [7]. Dynamic recovery method is unable to tolerate such sort of faults. Moreover for safety-critical applications operated in real-time, dynamic reconfiguration cannot be used because it requires extra time for testing and reconfiguration prohibiting its uses in real-time fault tolerance. In such cases, static methods are always preferred for its capability of immediate masking of errors. But most of the existing static methods suffer from the limitation of large area overheads [8] which restrict to use them in resource constrained applications [9]. Sometimes only the critical portions of a system are made fault tolerant first to increase hardware usage efficiency and, at the same time, to minimize area overhead [10].

In this paper, we propose a new static fault tolerant method, viz. triple transistor (TT) redundancy method, which offers a good reliability at lower hardware complexity compared to the existing static methods making it suitable for designing fault tolerant systems in today's resource constrained applications. This technique is completely based on the redundancy at transistor level and hence offers higher reliability for the designs compared to techniques where redundancies are added at higher level of abstractions (gate level or block level) [11]. Theoretical as well as simulation results have been provided to highlight the attributes of our design. Proposed TT method requires large critical path limiting its use in high speed systems and in such cases, we may use the TT method in making some parts of them fault tolerant.

## 2. Previous works

In early 50s, von Neumann proposed a new fault tolerant approach based on NAND multiplexing [12], where each gate of the circuit implemented using NAND gates is replicated for $N$ times and inputs and outputs are formed using bundles of $N$ lines, proper interconnections among which assures extensively high reliability for the circuit. But practical application of the technique is limited by the inherent assumptions of very low gate error rates and huge amount of redundant components. Some extended versions of the multiplexing techniques are $N$-tuple modular redundancy (NMR) [13], interwoven redundant logic [14], quadded logic (QL) [15] etc., each of which has their own advantages and applications. In case of NMR, the circuit modules are $N$-

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plicated, i.e. copied for N-times, perform the same computations and a majority voter at the output detects the correct output provided that at least ($\lfloor\frac{N}{2}\rfloor + 1$) modules are fault-free. Special case of NMR is triple modular redundancy (TMR) [16] where three identical modules perform the same job and an output majority voter compares the results to select the final output. In general output majority voters are assumed to be robust, which is not practical. Indeed, voter is the decision making part in TMR and hence failure of it produces incorrect outputs. In [17], the authors have used a dual to TMR where one of the modules in a TMR system is in sleep mode and gets activated upon finding a mismatch in the outputs of the other two operating modules.

QL technique is better than TMR in terms of reliability and critical path, but requires almost eight times of area compared to the non-redundant one and takes upto two subsequent levels to absorb an error making it inefficient for circuits with small logic depths. Sometimes majority voters are used at the outputs to select the final output from the quad, but includes the problems with the unreliable voters. A more cost-effective solution over QL in the above respects is quadded transistor (QT) logic proposed by El-Maleh et al. in [18], where each transistor of the circuit under consideration is quadded. More concept of quadding the components to increase the circuit reliability were previously discussed in [1,19]. In case of QT, each transistor in the circuit is replaced either by parallel connection of two pairs of transistors connected in series or by series connection of two pairs of transistors connected in parallel (as shown in Fig. 1). For normal fault-free operation, quadded inputs get identical values as that of the original input in the case of a single transistor. It is obvious from the structures 1*b* and 1*c* that the failure of a single transistor in the fault tolerant QT does not affect the functionality of the original circuit. The arrangements also have the capability to tolerate multiple faults affecting a particular set of transistors.

Gate capacitances of the QT logic are quadrupled due to the replacement of every transistor with quad structure and hence the system becomes quite slow and power consuming, which makes the method non-favourable for practical designs. To accelerate the system speed, the size of the transistors can be increased, but that in turn would increase the area overhead of the overall design. Feeding each of the quadded inputs of single transistor separately from single output of the previous level makes the interconnections quite cumbersome. To reduce the problem, quadded gates at each level can be quadrupled to generate four separate outputs and feed the next level inputs of the QT [20] gate. But such design requires impracticable hardware overhead which has been sorted out in Gate-specific QT (QT8) based SEU mitigation technique, where connection to the specific inputs of a quadded gate is made from two copies of the quadded gates at the previous level, minimizing the total number of transistors by half. But such design still requires about eight times of area compared to the non-redundant one. In TMR-QT method [21], QT is used to design the voters in TMR and provides very good circuit reliability. But because of the quadded structure of the majority voter, this method requires large area as well as delay overheads. It is also quite cumbersome to feed the quadded inputs of the voter from three outputs of the triplicated modules of TMR.

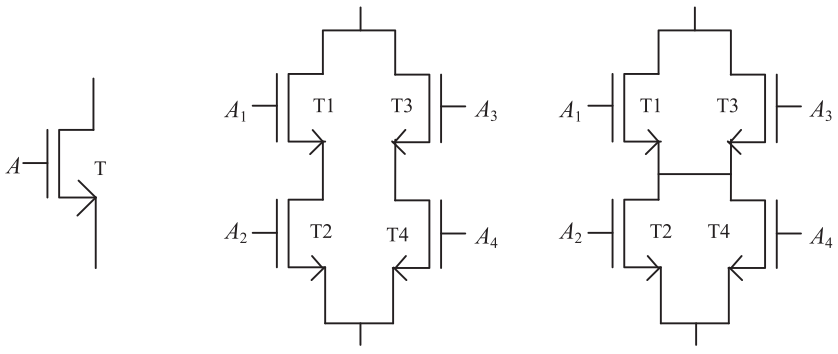
A generalized modular redundancy scheme for enhancing fault tolerance of combinational circuits has been proposed in [22]. Fault tolerance based on selective-transistor redundancy has been proposed in [23]. In quad-gate-transistor (QGT) [24] method, the authors have merged redundancy at gate level with redundancy at transistor level, where the gates at the last stage of the QL implementation of a circuit are replaced by QT arrangement making it more hardware efficient compared to QL and much faster than QT method. But because of its large hardware overhead and complex interconnection topology in the QL part, QGT method is quite area and power hungry which increases a lot for larger circuits. Sometimes error in one group in the QL part of QGT may spread to more than one gates at different groups in the next level leading to complete circuit failure.

The above discussions show that all the existing static fault tolerant methods either require considerable high area overhead or introduce large delay in the circuit limiting their usage in practice. For resource constrained applications like satellites, avionics and today's microcomputer systems, where increase in payload is a major concern, we cannot use these methods to increase the reliability of a system and must look for some alternatives [25]. Our proposed TT technique requires much lesser area overhead compared to all other existing methods and also shorter critical path than QT. Hence it can be used in resource constrained applications where area cannot be compromised for the sake of reliability.

## 3. Proposed TT method

### 3.1. Fault model

Static fault tolerant methods can tolerate all sort of errors, permanent or transient in nature. In our proposed method, we have considered both types of transistor defects: stuck-on and stuck-off. Transistor stuck-on and stuck-off faults respectively imply the permanent closing (short) and opening of the path between the source and the drain of a MOSFET [26]. Therefore in practice, stuck-close faults behave and is modelled as stuck-on faults, whereas stuck-open faults are similar to and hence modelled as transistor stuck-off faults. Input stuck-at-1 (s-a-1) fault to the gate terminal of an *n*-MOS transistor causes permanent closing of the path between drain and source of it, which corresponds to the transistor stuck-on fault. Input stuck-at-0 (s-a-0) fault to an *n*-MOS transistor results in open in the path between drain and source causing transistor stuck-off fault. Similarly, input s-a-1 and s-a-0 faults at the gate of a *p*-MOS transistor can be modelled as transistor stuck-off and stuck-on faults respectively and vice-versa. Hence, any gate level stuck-at fault at the input stage of the TT logic is modelled as transistor level defect for ease of fault analysis.




(a) Original Transistor (b) QT version 1 of Fig. a (c) QT version 2 of Fig. a

**Fig. 1.** QT structure of single transistor.