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A new approach to frequency-domain noise analysis and design of a very-low noise amplifier in radio and microwave frequencies

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ABSTRACT

This work presents a new idea to design and optimization of noise with a very-low-noise amplifier (VLNA). Noise optimization is done using suitable filters. An appropriate filter can convert circuit noise frequency response into a band stop. This is while the amplifier gain is in bandpass state. Hence, suitable gain and minimum noise are achieved in band pass. Using this approach in 0.13 μm CMOS technology, a VLNA in the frequency range of 20–1000 MHz is designed with the following specifications: minimum noise figure 0.95 dB, transfer gain 15.39 dB, third order intercept point −15.2 dBm at 900 MHz, die area of 0.075 mm^2, and power dissipation of 18.16 mW. To our knowledge, by comparison with recently reported LNAs, the presented LNA achieves the highest figure of merit (FOM) by taking into account the NF.

1. Introduction

Implementation of very low noise and high-frequency amplifiers in CMOS technology is possible as per following methods: 1) Conventional noise matching, 2) simultaneous noise and impedance matching at input [1,2]) power-constrained noise optimization, for example, by transistor sizing at the first stage [3], 4) power-constrained simultaneous noise and input matching, for example, by paralleling gate and source nodes of MOSFET [4], and 5) tuning of signal source impedance [5], for example, by selecting a desired value of source impedance, noise of common source amplifier can reach minimum noise of amplifier. In the above methods of noise optimization, two main issues should be considered: operating point of the circuit and noise matching.

In this work, we want to take into account noise frequency response and change it using appropriate filters. This means that for a bandpass amplifier, noise frequency response is changed from allpass to bandstop. The noise energy from the bandpass would be moved to the sidebands to minimize the noise in a bandpass. Only the thermal noise is considered here.

In Section 2, the noise performance of common-source low noise amplifiers is investigated. According to the approach of Sections 2 and 3, a new low noise amplifier circuit is proposed at the beginning of Section 4 and frequency response of the circuit gain is derived. Then, a very accurate noise analysis of the circuit is presented at the second parts of Section 4. Consequently, in Section 5, an accurate design approach is used based on the square value of transconductance transfer function that is the most important factor in noise analysis. The layout of the circuit and post-layout simulation results are presented in Section 5. Also, the circuit performance is compared with other reported amplifiers using a table. Ultimately, the conclusion is presented in Section 6.

2. Overview of low noise amplifier circuits, high-frequency noise

First stage conventional structures for low noise high-frequency amplifiers are shown in Fig. 1. Noise figure for each structure except Fig. 1-(d) is given in the following. The noise figure of Fig. 1-(d) will be calculated later in Section 4.

2.1. Noise figure of the resistance terminated circuit

To extract the noise factor of circuit Fig. 1-(a), it is redrawn in Fig. 2. In this figure thermal noise of R_S is:

$$\overline{v_{n,R_S}^2} = 4kTR_S\Delta f \rightarrow \overline{i_{n,R_S}^2} = \frac{4kT\Delta f}{R_S} \quad (1)$$

the thermal noise of R_g is:

$$\overline{v_{n,R_G}^2} = 4kTR_G\Delta f \rightarrow \overline{i_{n,R_G}^2} = \frac{4kT\Delta f}{R_G} \quad (2)$$

the thermal noise of r_g is:

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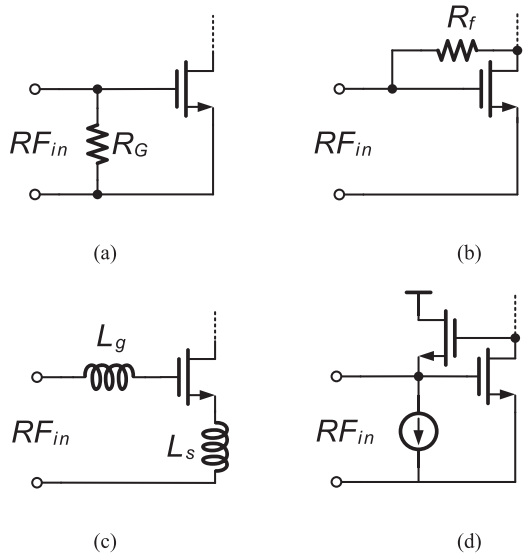

Fig. 1. Conventional common-source LNA structures: (a) resistance terminated, (b) shunt-shunt feedback, (c) series gate and source degeneration inductance, and (d) active feedback.

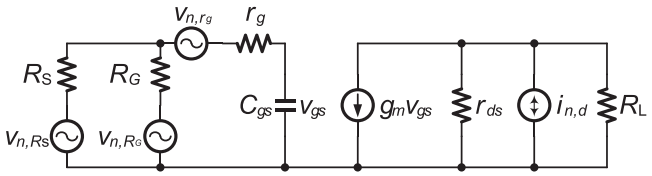

Fig. 2. Equivalent circuit of Fig. 1-(a) for calculating noise factor.

$$\overline{v_{n,r_g}^2} = 4kTr_g\Delta f \rightarrow \overline{i_{n,r_g}^2} = \frac{4kT\Delta f}{r_g} \tag{3}$$

and

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0} \tag{4}$$

is the channel thermal noise. In recent relations k is the Boltzmann constant, T temperature in terms of Kelvin, Δf is bandwidth of noise in Hz, γ is the noise factor related to operating point which for the transistor with a length larger than 1 μm is in the interval of $2/3 \leq \gamma \leq 1$, for the transistor with a length less than 1 μm is between 2 and 3, and g_{d0} is channel conductivity when drain-source voltage is equal to zero. If the transistor is in strong inversion, then, it can be assumed that the ration of g_m to g_{d0}, which is chosen as α, is close to 1, as reported in many papers [6,7]. The parameter r_g is the gate series resistor of the transistor. Both parameters γ and g_{d0} are increased with the increase of V_{GS} and V_{DS} [8]. For $\Delta f = 1$Hz, according to the Fig. 2, noise factor of Fig. 1-(a) is:

$$F(f) = \frac{R_G}{R_G + R_S} + \frac{r_g}{R_S} + \frac{\gamma g_{d0}}{R_S G_m^2} \tag{5}$$

In the recent equation, R_G is gate bias resistance, R_S is the impedance of the input source, r_g is equivalent gate series resistance, and $G_{m,T}$, the total transconductance of the circuit, is derived as follows:

$$G_{m,T} = \frac{g_m R_G}{j\omega C_{gs}(R_S R_G + r_g(R_S + R_G)) + R_S + R_G} \tag{6}$$

After some simplifications in terms of $\alpha = g_m/g_{d0}$ and $\omega_T = g_m/C_{gs}$, and by assuming $R_S >> r_g$ the following is achieved:

$$F = 1 + \frac{R_G}{R_S} + \left(\frac{\gamma}{\alpha}\right) g_m R_S \left(\frac{\omega}{\omega_T}\right)^2 \tag{7}$$

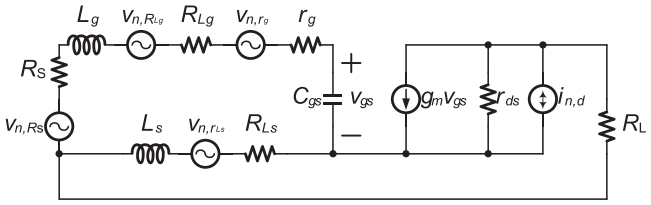

Fig. 3. Noise equivalent circuit of Fig. 1-(c).

2.2. Feedback circuit parallel-series noise figure

Circuit noise factor of Fig. 1-(b) with respect to a load in the drain of the transistor, can be obtained as follows [1]:

$$F = 1 + \frac{R_F}{R_S}\left(\frac{1 + g_m R_S}{1 - g_m R_F}\right)^2 + \frac{1}{R_S R_L}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 + \frac{\gamma g_m}{\alpha R_S}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 \tag{8}$$

The amplifier gain also includes:

$$A_v = R_L \frac{1 - g_m R_F}{R_F + R_L} \tag{9}$$

According to two recent relations, there is a trade-off between the noise and gain. Noise attenuation entails for gain loss. Noise factor of this structure in the technology of 0.18 μm CMOS is about 4 dB [9].

2.3. Noise figure of the common-source circuit with source degeneration

The noise factor of the circuit of Fig. 1-(c) is the same as a conventional common-source circuit, i.e. Fig. 1-(a). Noise equivalent circuit of Fig. 1-(c) is illustrated in Fig. 3. Eliminating noise of source inductance, after some calculations, noise factor is obtained as follows:

$$F = 1 + \frac{r_g}{R_S} + \frac{\left(\frac{\gamma}{\alpha}\right) g_m}{R_S}\left(\frac{\omega_{in}}{\omega_T}\right)^2 (r_g + R_S)^2 \tag{10}$$

where r_g is equivalent noise resistance of the gate, $\alpha = g_m/g_{d0}$ and $\omega_T = g_m/C_{gs}$ is the cut-off frequency of input terminal. The recent equation is obtained at the frequency of ω_{in} by assuming $\omega_{in} = 1/\sqrt{(L_g + L_s)C_{gs}}$ and $\omega_T L_s = R_S$. If $R_S >> r_g$, then noise factor can be simplified as:

$$F = 1 + \frac{r_g}{R_S} + \left(\frac{\gamma}{\alpha}\right) g_m R_S \left(\frac{\omega}{\omega_T}\right)^2 \tag{11}$$

which F is the same as basic common-source noise factor. Upon taking a derivative of noise factor with respect to R_S, the optimum value of the source resistance, i.e. R_S, and the amount of the minimum noise factor is obtained:

$$R_{S,opt} = \frac{\omega}{\omega_T}\sqrt{\frac{r_g}{\left(\frac{\gamma}{\alpha}\right) g_m}} \tag{12}$$

$$F_{min} = 1 + 2\frac{\omega}{\omega_T}\sqrt{\left(\frac{\gamma}{\alpha}\right) g_m r_g} \tag{13}$$

But the main advantage of this structure over basic common source structure is the full matching established with gate and source inductances. Inductor at the source node of transistor creates a real resistance of $g_m L_s/C_{gs}$ at the input, thus eliminating the effect of gate-source capacitance, i.e. C_{gs}, by means of two inductors L_s and L_g, and creating a real resistance by L_s, there is the possibility of complete input matching at the resonant frequency of $\omega_{in} = 1/\sqrt{(L_g + L_s)C_{gs}}$. In addition, to improve the noise performance a capacitor can be used in parallel with gate and source nodes [2].