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A high output swing current-steering DAC using voltage controlled current source

Qinjin Huang[a,b,c], Fengqi Yu[a,b,c,*]

[a] Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen University Town, 1068 Xueyuan Avenue, Shenzhen, China
[b] University of Chinese Academy of Sciences, Beijing, China
[c] Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China

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ABSTRACT

As the supply voltage decreasing to near 1 V, the output swing of the CS-DAC (current-steering digital-to-analogue converter) is limited by the minimum biasing voltage of the current source array, which is approximately 0.4 V. This voltage takes one-third of the 1.2 V power supply, which makes the single-ended CS-DAC not practical. To eliminate the output swing limitation, a voltage-controlled current source (VCCS) is proposed to realize high-swing single-ended voltage output for CS-DAC. The VCCS has the same input voltage as the biasing voltage. It generates a matching output current to make the minimum output voltage of the single-ended CS-DAC be able to reach the ground. The VCCS adopts a cascode structure in the output path, thus its performance is independent of DAC output changes. Careful matching is made inside VCCS, as well as between VCCS and DAC. Consequently, this design is robust to the process, supply voltage, and temperature (PVT) variations. The proposed CS-DAC, implemented by 180-nm CMOS technology, has a 1 V output swing under 1.25–1.5 V power supply at 25 °C temperature. For all PVT variation corners, the measured minimum DAC output voltage, designed as 0.11 V, varies between 0.05 V and 0.113 V. The measured DNL and INL are normally less than 0.2 LSB and 0.5 LSB, respectively. The measured slewing time for rising and falling step input are 80 ns and 90 ns, respectively. The measured total power consumption is 1.5 mW.

1. Introduction

Battery powered equipment generally demands single-supply-rail devices. These single-supply-rail devices have single-ended signal port rather than differential port. At the same time, supply voltage is declining to 1.5 V, and even to near 1 V. When the supply voltage is low, it is critical for single-ended voltage in/out ports to have high-swing or full-swing range, otherwise the signal swing is too small. Besides, power consumption is a key parameter for portable systems. As an important interface device, DACs operating at low power supply voltage with high-swing and low-power consumption are one of the research focuses.

To generate high-swing single-ended voltage output, resistor-string DAC (RS-DAC) is commonly used [1–3]. The conventional structure of RS-DACs is shown in Fig. 1(a). The RS-DACs have advantages including monotonicity, low power, and full output range from ground to reference voltage. It is applicable for low-resolution and low-speed applications. However, for resolution greater than 10-bit, the voltage-select switches and the resistor units grow exponentially with the resolution number, leading to a large RC delay and a large die size. As a result, RS-DACs are used in speed lower than several mega samples per second, not available in higher resolution and higher speed applications.

Comparing to RS-DACs, current-steering digital-to-analogue converters (CS-DACs) are naturally appropriate for high-resolution and high-speed applications. This is because current source has fast charging speed, small switching-delay, and independent of the number of bits of DAC. To achieve high-speed, CS-DACs are commonly configured in differential scheme, as shown in Fig. 1(b) [4]. In this way the differential CS-DAC's speed is not limited by the output amplifier. When CS-DAC is adopted in single-end applications, each of the differential outputs is available for single-ended voltage output. For single-ended voltage output, there exist two problems. One is its linearity performance suffering from finite output resistance of the current source unit [4]. The other is that the output swing is limited because the minimum saturation voltage of current source unit cannot be neglected under single power supply around 1 V.

The first problem, limited output resistance, can be resolved traditionally by adding an operational amplifier at the output, together with a feedback resistor, as shown in Fig. 1(c). In this way the voltage at the

* Corresponding author.
E-mail addresses: huang.qj@siat.ac.cn (Q. Huang), fq.yu@siat.ac.cn (F. Yu).

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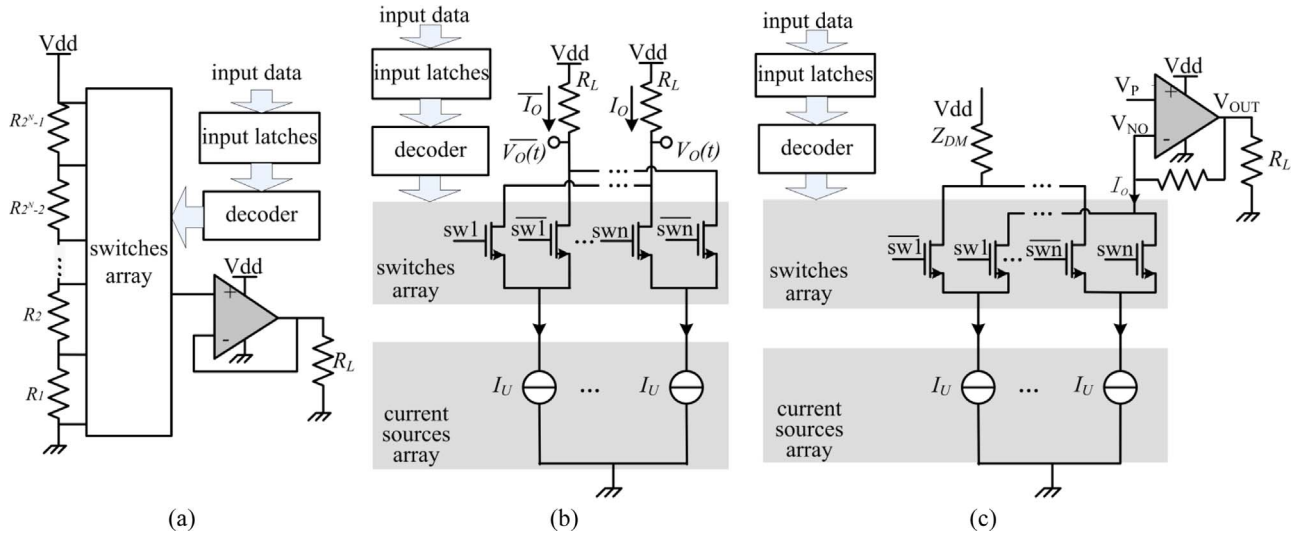

Fig. 1. Traditional single-ended DAC. (a) The conventional structure of RS-DACs. (b) The CS-DACs driving resistant load without output amplifier. (c) The CS-DACs driving load by a single-ended output amplifier.

output of current-steering array is constant so that its linearity improves. This configuration is applicable for medium speed applications because the OP generally operates at lower speed than that of the current-steering array. Although CS-DAC with OP reaches compromise between speed and linearity, it is still hardly used in the applications demanding single-ended voltage output under low supply voltage [1]. The reason is that it still suffers from swing limitation [2].

The second problem, limited output swing, is more crucial for low voltage applications and causes great attention. Przyborowski and Idzik adopted an extra current mirror with traditional current-steering array and output-amplifier to eliminate the swing limitation and accomplish a high-swing output for single-ended voltage-output CS-DAC [5]. In their work, the extra current mirror is used to change the current direction from sourcing to sinking when the most-significant-bit (MSB) switches. However the current mirror has a limitation of a small current range which was 0.05 mA in their work. In addition, it introduces two problems. One is the possible mismatch of the extra current mirror in the MSB, leading to more stringent matching requirement. The other is that the current mirror decreases the full-scale switching speed because of the extra settling time caused by full current swing in the current mirror. Therefore the full-swing CS-DAC with an extra current mirror is mainly suitable for low-speed (< 1 MHz) applications. Park and Song proposed a full-swing CS-DAC consisting of a PMOS and a NMOS current source array, with a quaternary driver and without using output amplifier [6]. So it has a pro of high speed (up to 1 GHz). However it has two shortcomings. One is that the two current source arrays double not only the die size, but also the power consumption. The other is the mismatch and inconsistency between the two current source arrays. So the full-swing CS-DAC with a quaternary driver is generally used in high-speed (up to hundreds MHz) and high-power ($>$ tens mW) applications.

To resolve the problem of limited output swing of the traditional CS-DAC with output-amplifier, as shown in Fig. 1(c), we propose a VCCS to generate a biasing current which directly eliminates the effect of the bias voltage for current source array. The proposed CS-DAC achieves high-swing output voltage by adding a small amount of power consumption and die area. Robustness has been considered in our proposed design. The extra VCCS do not affect the nonlinearity and dynamic performance of the previous CS-DAC. The main contribution of our work is to fill the gap between high-power high-speed CS-DAC and low-power low speed one, i.e. for the applications of medium speed (up to tens MHz) and relative low power (1–2 mW). To the best of our knowledge, we have found very few publications on such topic.

The rest of the paper is organized as follows. In Section 2, swing limitation of single-ended voltage-output CS-DAC is discussed. Section 3 describes the design of the proposed high-swing DAC. The measurements, together with comparison among state-of-art full-swing DACs, are presented in Section 4. Finally the conclusions are given.

2. Swing limitation of single-ended voltage-output CS-DAC

Single-ended voltage-output CS-DAC generally adopts the scheme shown in Fig. 1(c). In this scheme, the output operational amplifier (OP) and feedback resistor are used as I-V converter and drive the load. The feedback resistor R_{FB} and the current steering block connect to the negative input V_{NO} of the OP. The positive input voltage V_P of the OP is a bias voltage that sets the current sources in saturation region. In this way, V_P defines the minimum output voltage of the DAC which is given in Eq. (1).

$$V_{OUT} = I_U \times (2^{N-1} \times b_{N-1} + 2^{N-2} \times b_{N-2} + \ldots + 2 \times b_1 + b_0) \times R_{FB} + V_P \quad (1)$$

For two-transistor-cascode current source, the minimum biasing voltage V_P is two times of the overdrive voltage, approximately 0.4 V in 180 nm CMOS technology. In other words, the minimum output voltage of CS-DAC is 0.4 V [9]. It is about one-third of the supply voltage which is around 1.2 V. Consequently, the single-ended CS-DAC is not practical for such applications. To solve this problem, we propose a technique to lower the minimum output voltage to accomplish a high-swing CS-DAC.

3. The proposed high-swing DAC

In this section, a high-swing DAC is proposed. We will discuss the architecture of the high-swing CS-DAC with a VCCS. In addition, the design detail of the VCCS will be described and its mismatch will be analyzed.

3.1. Architecture

To expand the swing range of single-ended voltage-output CS-DAC, this paper adopts a VCCS to generate a biasing current I_B. This current is injected into the negative input node of the amplifier and the difference between I_B and I_O flows through the feedback resistor, as shown in Fig. 2. In this way, a voltage drop is generated from V_{NO} to V_{OUT}. This voltage drop is designed to match the biasing voltage V_P of the current-steering sources. When they match accurately, the minimum output