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A 0.3 V 8-bit 8.9 fJ/con.-step SAR ADC with sub-DAC merged switching for bio-sensors

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ABSTRACT

An 8-bit 10 kS/s 0.3 V ultra-low power successive approximation register (SAR) analog-to-digital converter (ADC) is proposed. On account of the presented sub-DAC merged switching scheme reducing the switch energy by 98.4% compared with conventional switching architecture, the energy consumption of the SAR ADC is decreased drastically. Furthermore, a presented double-bootstrapped switch with leakage reduction technologies improves sampling linearity under 0.3 V. In addition, to relieve non-linearity, boost technique is introduced in digital-to-analog converter (DAC) driving switch. The proposed ADC has been fabricated in 180 nm 1.8 V CMOS process. The measurement results show that effective number of bits (ENOB) of the ADC is 7.21 bit at the Nyquist input frequency and 0.3 V supply voltage, achieving a figure-of-merit (FOM) of 8.9 fJ/conversion-step. The chip area is 0.084 mm^2.

1. Introduction

The demands on emerging electronic systems with restraint energy budget such as wireless sensor networks, energy-harvesting systems and battery powered mobile devices have been rapidly increased. Meanwhile, portable diagnosing equipment, pacemakers, pulse oximeters, electrocardiographic (ECG) and electroencephalograph (EEG) monitoring systems need to stay on all time to monitor and store patients' vital data. Such devices are often powered by energy harvesting circuits, driving extensive research on circuit technologies for micro-powered SoCs [1–3]. As a mandatory block in the analog front end of such devices, ultra-low power and operating frequency ADCs becomes extremely worrying. Recently, ultra-lower power ADC used for sensor interfaces and wireless sensing applications have been presented in [4,5]. Furthermore, some ADCs suitable for low voltage power supply have been reported so far in [6,7].

In many ADC architectures, SAR ADC has become a mainstream research topic due to the simple structure so that the SAR ADC is very suitable for circuits supplied by power harvesters. The power consumption of the digital circuit block decreases with the reduction of the power supply voltage. However, most analog circuit blocks such as S/H switch and comparator are hardly turned on with ultra-low supply voltage and high V_{th}. Moreover, the leakage currents contribute to a significant portion of the total power consumption with the decrease of the supply voltage. In addition, to reduce the overall power consumption of a SAR ADC, many researches have shown interests in improving the DAC switching sequence. Compared to the conventional architecture, the set and down [8], V_{cm}-based [9], sub-DAC merging [10], hybrid capacitor switching scheme [11] and energy-efficient switching method [12] for an 8-bit SAR ADC reduce the switching energy by 81.2%, 87.5%, 96.8%, 98.83%, 99.32% respectively.

The SAR ADC in [13] achieves 78.4 nW and 5.2 ENOB at a sampling rate of 17.8 kS/s which has a FOM of 119.8 fJ/conversion-step. An 8-bit single-ended SAR ADC which achieves 7.4 ENOB and 63.4 fJ/conversion step FOM is presented in [14]. However, the operating voltage as high as 1.1 V restricts its application. Background self-calibration technique of comparator offset is realized in [15], which can obtain 5.04 fJ/conversion-step at 0.35 V supply voltage. The ADC presents a power consumption of 146 nW at the sampling rate of 20 kS/s [16]. SAR ADC presented in [17] operates at 0.3 V supply voltage and 5 kS/s sampling rate, achieving a FOM of 7.3 fJ/conversion-step. The supply-boosted time-domain comparator enhances the operation speed of the latch in ultra-low voltage. However, the extra supply-boosted circuits and capacitors increase the total power and complexity.

In this paper, we present a DAC switching scheme which shifts the common-mode level near to V_{ref} to make the dynamic comparator work well in ultra-low supply voltage. Modifying the architecture in [10], the presented scheme achieves a reduction of 98.4% and 75% in the switching energy and area, compared to the conventional one. In addition, the control logic is very simple and the number of the switches is less than the conventional scheme for an 8-bit SAR ADC. Substrate bias technique and stacked transistors are employed in the double-boosted

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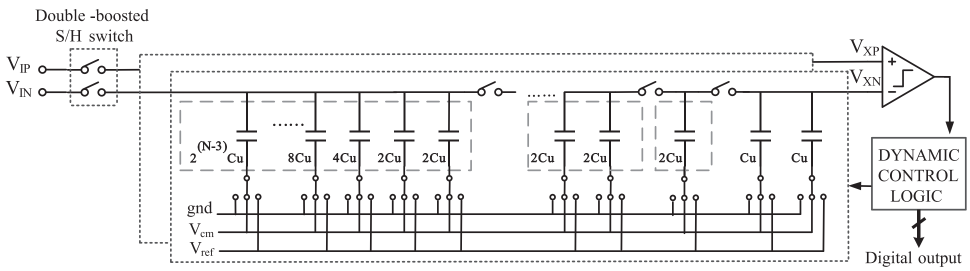

Fig. 1. Block diagram of the proposed SAR ADC architecture.

S/H switch to reduce the leakage current. Furthermore, due to the small parasitic capacitors in the gate of the switches, the linearity of the proposed switch network is better. In ultra-low voltage design, dynamic range of the comparator is limited by voltage headroom. To facilitate ultra-low voltage operation, a bulk-driven based fully dynamic comparator is used.

This paper is organized as follows: in Sections II, the sub-DAC merged switching method of the proposed SAR ADC is described; Section III provides the design and implementation considerations; in Section IV, measurement results are shown and compared with low-power competitors followed by conclusion in Section V.

2. Proposed SAR ADC architechture

2.1. Energy analysis

Fig. 1 shows the complete block diagram of the proposed ADC. The fully differential architecture is employed to suppress supply voltage noise and have good common-mode noise rejection. In this paper, a new sub-DAC merged capacitor array structure is presented, which improves the switching energy by 98.4% and reduces the DAC capacitor area by 75%, when compared with the conventional scheme. In addition, the proposed switching architecture shifts the common-mode level to V_{ref}, which makes the dynamic comparator work well in ultra-low supply voltage. The presented switching scheme divides the 2^iC_u ($i > 1$) in the conventional capacitor arrays into binary-weighted capacitors, with the unit capacitor of $2C_u$.

Fig. 2 presents the DAC switching architecture for a 5-bit SAR ADC. The switching scheme is realized in four phases: most significant bit (MSB), 2nd-MSB, 3nd-MSB to 2nd-LSB (second least significant bit) and LSB. In the first phase, the differential input signal is sampled on the top-plates of both capacitor arrays, and the bottom-plates of capacitors are initially connected to gnd. After sampling the input signal, the bottom plates of the capacitors are switched to the common-mode voltage V_{cm}, which is $0.5V_{ref}$, changing the input common mode voltage from V_{cm} to V_{ref}. Then, all the switches splitting the capacitors are turned off and the MSB is obtained. In the second phase, the SAR logic will switch the bottom-plates of the main-DAC capacitors which sample the higher input voltage to gnd and the other main-DAC capacitors remain unchanged. Then the 2nd-MSB is obtained. In the third phase, the sub-DAC utilizes all the previous bits to generate the next reference voltage. The positive and negative reference voltages on the V_{XP} and V_{XN} side are shown in Table 1. Then this sub-DAC merges with the main-DAC and becomes a part of it. This procedure continues until the 2nd-LSB is determined. In the LSB phase, the dummy capacitors are used to determine the last bit based on the MSB and 2nd-LSB. Table 2 shows the conversion mode of two dummy capacitors.

As shown in Fig. 2 compared with [10] this switching architecture wastes no energy in the first two steps. Only one dummy capacitor is switched to determine the LSB, resulting in less switching activity and lower energy consumption. In addition, the proposed scheme requires 2(N-9) more switches than the conventional structure. In other words, the number of switches in the proposed scheme is 2 less than that of the conventional one for an 8-bit ADC, which is our expectation.

For the proposed method, the switching energy required to generate the Mth (B_{M-1}) can be written as

$$E_M = \begin{cases} 0, & M = 1,\ 2 \\ \frac{1}{2^{M-1}} \cdot C_u \cdot V_{ref}^2, & M = 3 \\ \frac{1}{2^{M-1}} \cdot C_u \cdot V_{ref}^2 + \frac{1}{2}\left(1 - \frac{C_{V_{ref}}}{C_{Total}^{sub-DAC}}\right) \cdot C_{V_{ref}} \cdot V_{ref}^2, & M \in [4,\ N-1] \\ \frac{1}{2^M} \cdot C_u \cdot V_{ref}^2 + A \cdot \left(\frac{1}{2} - \frac{1}{2^{M-2}}\right) \cdot C_{V_{ref}} \cdot V_{ref}^2 + \frac{(-1)^A \cdot B}{2^M} \cdot C_u & M = N \\ \cdot V_{ref}^2, & \end{cases} \tag{1}$$

where $C_{V_{ref}}$、$C_{Total}^{sub-DAC}$、A and B are given by $C_{Total}^{sub-DAC} = 2^{M-2}C_u$

$$C_{V_{ref}} = \sum_{i=1}^{M-2} C_i \cdot (B_i \odot B_0) \quad A = B_{M-2} \oplus B_0$$

$$C_i = \begin{cases} 2^{M-2-i}C_u, & i \neq M-2 \\ 2C_u & i = M-2 \end{cases} \quad B = \sum_{i=1}^{M-3} 2^{M-2-i}(B_i \oplus B_0)$$

The comparison of a differential 8-bit SAR ADC based on previously published switching schemes and the proposed sub-DAC merged switching scheme are performed. Table 3 summarizes the features of different switching schemes for an 8-bit SAR ADC.

It can be seen that the proposed method is competitive with the current state-of-the-art. The average switching energies for the sub-DAC merging switch [10] and the proposed switch are $10.66C_uV_{ref}^2$ and $5.57C_uV_{ref}^2$ respectively. In [11], the calculated energy is only the power consumption in comparison phase and does not include the reset energy. The bottom of the capacitor is restored to original state when the current conversion is end for next sample, which will consume energy called reset energy. However, in the proposed scheme the reset phase, the bottom of the capacitor is connected with gnd, which don't consume energy in reset phase. So the presented scheme is competitive. The power reduction in [12] is obvious, however, the use of the bridge capacitor will reduce the linearity.

The successive approximation waveform is shown in Fig. 3. And the right slide curve in phase 6–8 is a zoomed in plot. As it is shown, the common mode level of two differential input is rose after sampling the input signal. The input common-mode voltage of is $3/4V_{ref}$ in phase 2. However, the difference between the inputs of comparator is large in phase 2, so the common-mode voltage will not affect the offset. In addition, the input common-mode voltage of is within the range from $7/8V_{ref}$ to V_{ref} after phase 2 which makes it possible to design a dynamic comparator operating at 0.3 V. This will be introduced in section III in detail.

2.2. Effect of the parasitic capacitors

Both the bottom and top plates of capacitors contribute parasitic capacitors, while parasitic capacitors of bottom plates do not affect linearity of ADCs, therefore, the analysis of the effect of top plates parasitic capacitors on linearity is discussed, as well as comparator input capacitor. As shown in Fig. 4, we take the digital code 10010 as an example, where C_{p1}、C_{p2} and C_{p3} are parasitic capacitors of sub-