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Leakage current elimination for Dickson charge pump with a linear regulator☆

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ABSTRACT

In this work, a Dickson-like charge pump has been adopted to obtain 30 V voltage for display driver integrated circuit applications. Meanwhile, an irreversible leakage current path in the traditional Dickson charge pump with a linear regulator is presented. This occurs normally when the regulated voltage level is too small to fully turn on its first auxiliary transistor, and then the first-stage Dickson charge pump is turned on all the time and consumes additional power. Three design technologies have proposed to address the power loss and simulation results have been used to verify the designs. Among them, a simple method, which utilizes the unidirectional conduction characteristic of a diode has been proven to be distinct for power saving and performance keeping by the silicon data. The total power consumption for the light load condition is halved for an input voltage of 2.9 V.

1. Introduction

CHARGE pump is one of the popular power management designs due to its attractive features such as magnetic-less structure, high efficiency and high integration [1]. Nowadays, many types of two-phase charge pump topologies, such as Dickson, series-parallel, Fibonacci, voltage doubler charge pumps [2–7], have been achieved. Among them, Dickson charge pump is more preferred for the on-chip power managements due to its smaller chip size and smaller power loss from parasitic capacitors. A pulse skip regulator is always added to obtain a stable output voltage [8,9]. It has fast transient response, but the output ripple is large in high current drive capacity applications. A linear regulator can be utilized to further improve the ripple performance [10,11].

However, a large reverse leakage current has often been witnessed in a traditional Dickson charge pump with linear regulation, especially in high power supply and light load condition. In this work, three control strategies have been proposed to fully cut off the leakage path for power saving with minimal performance loss. The silicon data reveals that the power consumption is halved for an input voltage of 2.9 V.

2. Reverse leakage current in Dickson charge pump with a linear regulator

Fig. 1 shows the traditional Dickson-like power system with a stable output voltage of 30 V for display driver integrated circuits, and its detailed principle is clarified in [10,11]. It is a power system with Voltage Conversion Ratio (VCR) of 20 and its related circuit parameters are shown in Table 1. Take the first stage of Dickson charge pump as an example to discuss its charge transfer. As is shown in Fig. 1(c), during the period T_3, $\varnothing_4$ changes from high to low, it turns on M_2 and allows C_{f2} to receive the charge from the preceding stage C_{f1}. During the period T_7, M_1 is turned on and C_{f1} is pre-charged.

One linear regulator is utilized to control the first three stages of the Dickson charge pump to be around 30 V. As shown in Fig. 1(b), $V_{REF} = 1.2$ V, and $V_{OUT,SERIES} = V_{OUT}/25$ is the feedback of V_{OUT} passing a voltage divider. The regulated amplitude of clock signal ($V_{OUT1,REG}$) is adaptive with different VCRs, V_{DD} and load conditions. With a higher VCR, V_{DD} or in a lighter load condition, the value of $V_{OUT1,REG}$ becomes smaller to weaken the output strength of the whole system.

Although a small output ripple can be achieved by the system, a large power loss can be introduced, which is a potential defect of this traditional Dickson scheme. Still take its first stage as the example. During the period T_7, C_{f1} is boosted and it begins to charge the next capacitor. Meanwhile, transistor M_1 is supposed to be fully turned off

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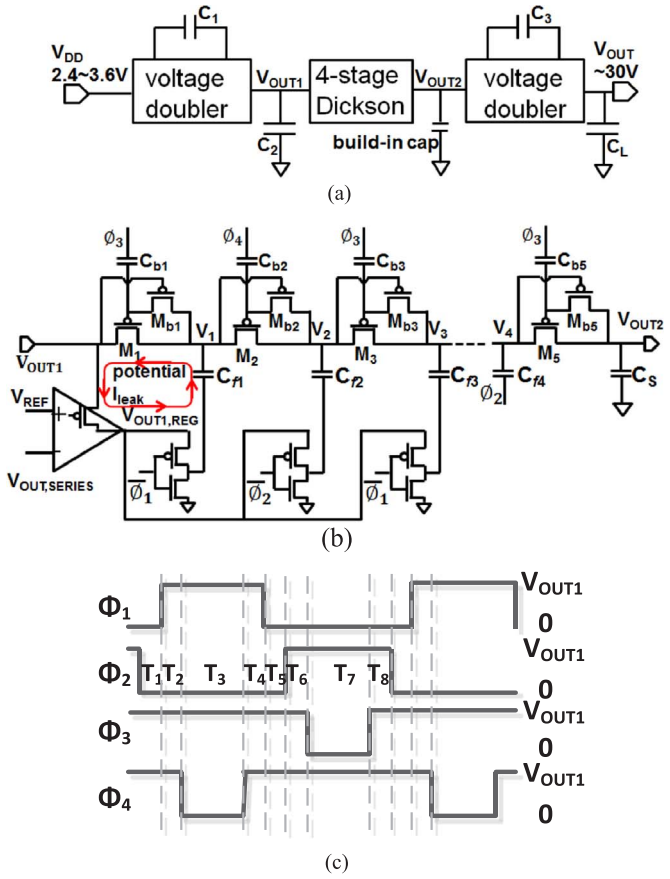

Fig. 1. (a) Power system with the traditional Dickson charge pump and (b) its feedback control with a linear regulator and (c) the related waveforms of driving clock.

Table 1
Circuit Parameters of the Mixed Charge Pump.

Parameters	1st voltage doubler	Dickson	2nd voltage doubler
Input voltage	2.4–3.6 V	4–6.6 V	~15.3 V
Output voltage	4–6.6 V	~15.3 V	30 V
Operation frequency	50 kHz	1 MHz	50 kHz
Flying capacitance	1 μF	450 pF for C_{f1}; 300 pF for others	0.1 μF
Storage capacitance	1 μF	400 pF	0.1 μF
Turn-on resistance of switching MOS	~10 Ω	~200 Ω	~200 Ω

with the help of the turned-on switch M_{b1}. However, for the power system with high VCR, V_{DD} or in a lighter load condition, the regulation loop decreases $V_{OUT1,REG}$ very much. In the worst case, if

$$V_{SG}(M_{b1}) = V_{OUT1,REG} < |V_{TH}(M_{b1})| \quad (1)$$

It leads to the situation where M_{b1} cannot be turned on anymore. Thus, the reverse leakage drawn in Fig. 1(b) introduces more power loss. Compared the subsequent stages, this situation is even worse in the first stage since the gate of M_{b1} is connected to a stable power supply V_{OUT1} and it is more likely to be turned off.

In our discussion above, PMOS is conducted as a transfer switch in the Dickson charge pump. If NMOS is used instead, just like the work in [12,13], it suffers this reverse leakage current as well, since the gate-drive of M_{b1} is the same as that shown in Eq. (1).

Fig. 2 shows the power consumption with VCR = 20 in the light load condition based on the silicon data. With the input voltage V_{DD} changing from 2.4 V to 3.6 V, the pump consumes current within

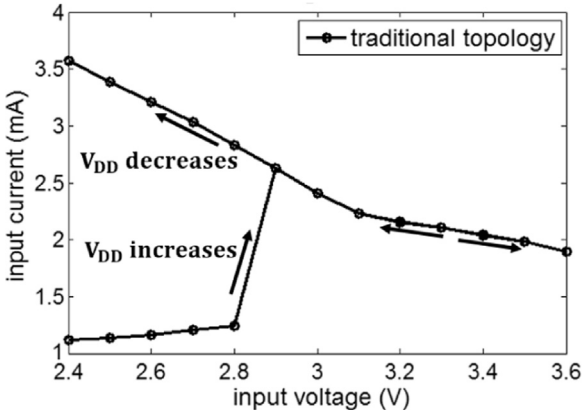

Fig. 2. The power consumption for the traditional Dickson charge pump with a linear regulator in the light load condition based on the silicon data.

1.2 mA for $V_{DD} < 2.8$ V, but the current increases rapidly when $V_{DD} > 2.8$ V. Since M_{b1} is never turned on for $V_{DD} > 2.8$ V and a negative voltage is stored in the capacitor C_{b1}, transistor M_1 will be always turned on with a large gate drive voltage V_{SG} , which introduces large power loss even if V_{DD} drops. This introduces hysteresis characteristic, as is described in Fig. 2. The power loss should be sensitive with the temperature and process corner, since it is related with the turn-on state of M_{b1}.

3. The proposed low power Dickson charge pump

To reduce the power loss, transistor M_1 in the first stage of the Dickson charge pump is required to be fully turned off during the phase $\varnothing_1$=1. One solution, named as c1, is to set transistor M_1 as diode-connected transistor. However, this design will introduce a voltage drop at the first stage.

The second solution is named as c2. We find M_{b1} has more chance to be turned off due to its small gate-drive. To avoid the voltage drop, the adopted linear regulator can be connected to regulate the 2nd–4th stages of the Dickson charge pump, instead of the first one. As is shown in Fig. 3, M_{b1} in this solution can be kept fully turned on since it has the large gate-drive voltage

$$V_{SG}(M_{b1}) = V_{OUT1} > |V_{TH}(M_{b1})| \quad (2)$$

The third solution c3 is shown in Fig. 4. As it reveals, the clock signal $\varnothing_2$ is connected to the gate of M_{b1}. During the phase when the flying capacitor C_{f1} is boosted, the voltage at the gate of M_{b1} has already dropped to 0 since the clock signals $\varnothing_1$, $\varnothing_2$ are complementary. Then, the gate drive of M_{b1} is set as (3), which fully turns on M_{b1}. Thus, M_1 is fully turned off rapidly.

$$V_{SG}(M_{b1}) = V_{OUT1} + V_{OUT1,\ REG} > |V_{TH}(M_{b1})| \quad (3)$$

The simulation results of the three solutions c1, c2, and c3, as well as the measured silicon data are given in the following section.

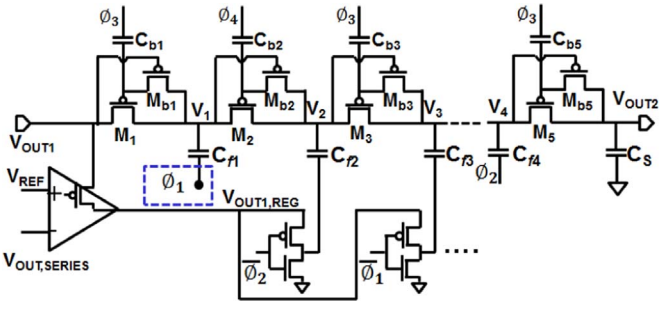

Fig. 3. Topology of solution c2, the proposed regulation strategy for reverse leakage current elimination in the first stage.