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A transient-enhanced low dropout regulator with rail to rail dynamic impedance attenuation buffer suitable for commercial design

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ABSTRACT

A low-dropout regulator (LDO) for portable application with a high output swing and dynamic biased impedance-attenuation buffer is presented in this paper. The proposed buffer pushes the dominated pole introduced by the LDO's power FET to higher frequency without consuming large quiescent current. The LDO loop with only one dominant pole within unity gain loop bandwidth is realized. A dynamic current sensing circuit is adopted to make the design more robust. The buffer features a rail-to-rail swing which makes the LDO's power FET size smaller than traditional buffer design for the same current deliverability. A low cost method for trimming is introduced to achieve high yield suitable for commercial design. The LDO has been fabricated in a 0.18 μm HV CMOS process. It draws a total current of 40 μA and is able to deliver up to 600 mA of load current. The proposed method for trimming allows for a high yield of approaching 100%, with line/load regulation error < 2%, and the maximum transient output voltage variation of 3% with a load step from 1 mA to 600 mA in 100 ns.

1. Introduction

POWER management system is playing a very critical role in all battery-powered systems, such as smart phones and tablets in order to achieve low standby current consumption and high power efficiency. The low-drop regulator (LDO) is one of the most critical modules in the power management system as it is used to regulate the rippled voltage supply to provide a “clean” voltage source for all kind of noise sensitive or level sensitive analog/RF/digital modules [1–5]. For commercial product development, it becomes very challenging to design a LDO with stable, low voltage drop, fast transient, and small area with an accurate output voltage under process-voltage-temperature (PVT) variations. Firstly, a large size power FET is needed for a LDO if the system requires a very low voltage drop across the power FET to achieve a better power efficiency. Secondly, it is essentially important for the LDOs with the specification of fast transient response and less voltage variation such as overshoot and undershoot to prevent the loading circuitry from being turned off or resetted abnormally. Thirdly, the LDOs with reasonable power supply rejection and output voltage accuracy are required if they are used as the supply of sensitive loading. These require a careful design with consideration of tradeoff among circuit topology, amplifier gain, silicon area and quiescent current etc [1,2].

A typical low drop-out regulator with an intermediate buffer stage is shown in Fig. 1. It consists of an error amplifier, a voltage buffer, a power pMOS in saturation region, a feedback network and an accurate voltage reference. The higher the LDO rated current, the larger the power FET size, which make loop stability design difficulty. Many solutions are reported to address the stability issues [2,6–8]. A properly designed buffer with low output impedance can move the power FET gate pole to a higher frequency. The design for the loop stability becomes simple because the loop stability is not affected by the power FET size. A dynamic biased super source follower (DB-SSF) is introduced in [8] to act as a buffer to drive the pMOS FET as shown in Fig. 2. The buffer's current biasing will track the output loading current in a wide dynamic range and enhance the slewing during transient between the different loadings.

However, DB-SSF might have some limitations during mass production. First of all, since the buffer is designed using pMOS source follower, it can provide turn-off voltage only for pMOS FET but cannot provide low enough output voltage (lowest buffer output voltage is ~ [Vgs + Vdsat]) to drive the power MOSFET with maximized over-drive voltage, such that a large pMOS power FET is necessary to deliver high current. It shows that the pMOS type buffer is not an optimized design for high current rating LDOs. The nMOS type buffer can maximize over-drive voltage for power FET so that it is a better choice for the LDO to deliver high current when silicon area is the concern. A buffer with rail-to-rail swing will make up the design defects of nMOS type buffer and

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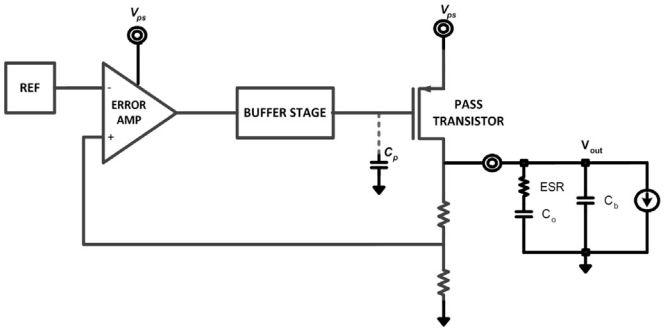

Fig. 1. Typical LDO structure with intermediate buffer stage.

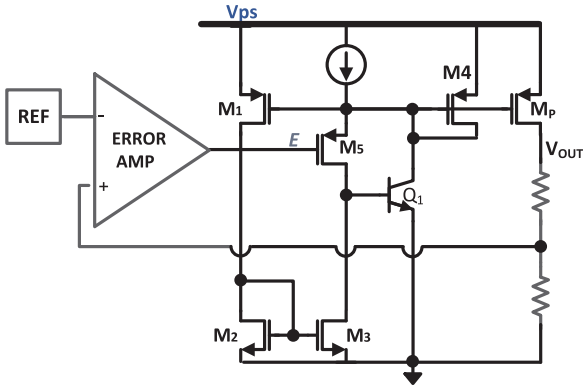

Fig. 2. LDO with intermediate dynamically biased buffer [8].

minimize the pMOS power transistor size. With the properly designed buffer, there are only two low frequency poles located at the error amplifier output and LDO output respectively. Since the parasitic capacitor at the error amplifier output node is minor, it will be much simpler to design a compensation circuit to this node pole for loop stability.

One compensation method is utilizing LHP (left hand plane) zero compensation [9–11], which provides a positive phase shift to compensate the negative phase shift generated by poles (leading phase compensation). One way of creating the LHP zero is to take advantage of the off-chip loading capacitor's intrinsic equivalent series resistor (ESR). However, the frequency of the ESR related zero is not well controlled due to the component variation and parameter degradation from off-chip component de-rating. Also, the zero frequency is not able to track the load condition which makes it difficult to purely rely on this zero for phase compensation.

Another way of having a LHP zero is to design an on-chip capacitor in series with a variable resistor at the error amplifier output node. Normally this series connected resistor can be designed to vary with load current so as to achieve phase compensation over a wide range of load conditions. The required large capacitor (due to no capacitor multiplication effect from Miller) will degrade LDO's non-linear dynamic performance such as slew rate, which is inversely proportional to compensation capacitor size and proportional to the error amplifier's input stage tail current. Extra current is needed for the error amplifier to improve the non-linear dynamic performance.

Another option for enhancing the loop stability is using either Miller or Ahuja compensation [12]. Comparing to Miller compensation, Ahuja compensation can provide wider loading capacitor range and a better power supply rejection (PSR), [12–15]. Specifically for Ahuja compensation design, the transconductance of cascode device should be designed at least a few times larger than the transconductance of the error amplifier's input pairs. The Ahuja compensated LDOs will have the bigger input referred DC offset voltage as compared to other type LDOs. There will be a design tradeoff between loop stability and input referred DC offset for Ahuja compensation scheme, which is one of the critical reasons for yield loss in the high volume commercial products. Another concern of DB-SSF is its current sensing circuit in term of robustness. In Fig. 2 the current of M4 can only track the output load current in first order. Due to transistor channel length modulation effect, the current sensing accuracy varies widerly with process-voltage-temperature (PVT) variations. Prediction of silicon behavior relying on simulation and foundry modeling accuracy can be a real concern when launching the same designed chip in different foundries.

In this paper, a rail-to-rail high swing super source follower buffer (RRHS-SSF) is proposed with the optimized minimun power FET size. To achieve a higher yield and more predictable performance, a more accurate current sensing circuit is proposed to generate the buffer's dynamic biasing as shown in Fig. 3. The designed LDO can deliver a current from micro-A to 600 mA. To minimize input referred DC offset, a trim scheme with minor engineering cost is introduced. Section 2 presents the principle of the proposed RRHS-SSF, and Section 3 discusses the compensation scheme, design parameters and presents the DC offset trim scheme as well. Finally, Sections 4 and 5 present the silicon measurement results and conclusion, respectively.

2. Proposed high swing impedance attenuation buffer

The most commonly used buffer is the single-stage source follower, which provides low impedance ($1/g_m$) at pMOS power FET gate with a

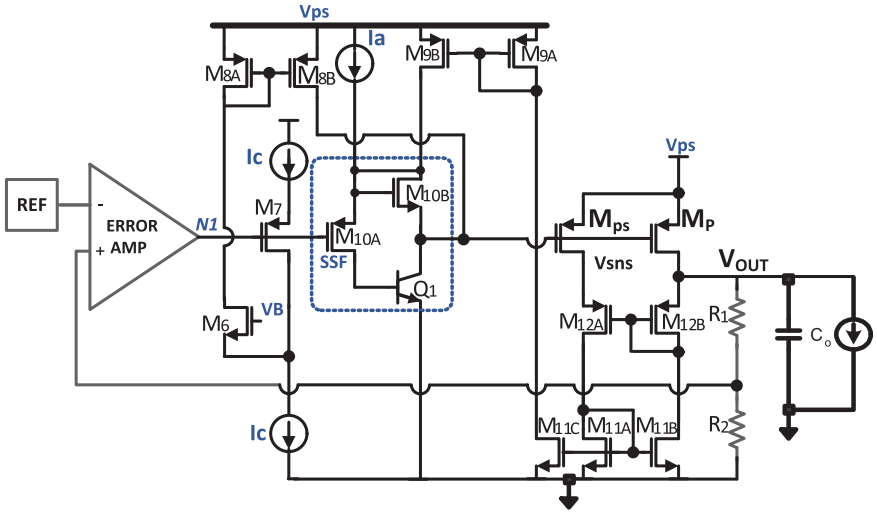

Fig. 3. LDO with proposed high swing super source follower buffer with dynamic biasing.