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Efficiency improvement of integrated synchronous buck converter using body biasing for ultra-low-voltage applications

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ABSTRACT

This article presents an integrated synchronous DC-DC buck converter for ultra-low-voltage and low-power applications with 200 mV–1 V input and 100 mV–500mV output in 45 nm CMOS technology. The proposed design uses over & under driving (OUD) and adaptive body biasing (ABB) methods to enhance the efficiency. In the proposed design, a control circuit with the least possible number of transistors is proposed which changes power MOSFETs threshold voltages adaptively depending on their operating modes by applying voltage to the body of the MOSFETs. The proposed method improves the conduction and switching losses simultaneously which achieves peak efficiency of 93%. The proposed converter has an acceptable performance and efficiency in sub-threshold voltages and also in the wide output current range.

1. Introduction

With the advances in CMOS technology and increasing demand for DC-DC switching power supplies in portable applications, there is a great demand for designing a low-power system-on-chip (SOC) power supply with high efficiency and tight regulation. In addition, these power supplies should provide the limits of the large scaling integrated (LSI) CMOS circuits design and fulfill the load demand.

One of the implementation limits of monolithic power supplies for analog and digital scaled-down size structures is decreasing their operating voltages to less than the threshold voltage for power saving applications. The power supply should be designed in such a way to provide a regulated ultra-low-voltage without increasing the design complexity and with acceptable efficiency.

In order to achieve the highest efficiency in high step down converters, the conduction and switching losses should be decreased. In scaling down size applications, excessive voltage drop on the circuit components would not only increase conduction losses, but also prevents the output voltage from reaching the desired value. Increasing the MOSFETs width could solve the mentioned problem and reduce the conduction losses but it also increases the switching losses and chip area. Besides, increasing the switching frequency to reduce the size of LC filter in DC-DC converters, would increase the switching losses. Therefore, an approach should be selected to enhance the efficiency by means of both conduction and switching losses improvement.

So far, different methods are investigated for integrated synchronous buck converter from different aspects such as, utilizing ZVS method to reduce the synchronous rectifier switching losses [1–3], energy recovery from circuit capacitor nodes and transferring this energy to other parts of circuit [1,3,4], using interleaved structure in order to increase current flow and reduce the size of the output filter [2,5], using stacked structure to reduce the output voltage ratio [6,7], presenting power management architectures in order to make a trade-off between the promising characteristics and converter area [8–10], using multi-phase converters in order to enhance power conversion efficiency [11,12], optimum output filter design to reduce the area and increase the quality coefficient [13,14], improving the gate drive circuit [15,16], designing optimum control system [17–23] and also using body biasing technique to improve the converter performance [24,25].

Generally, body biasing could be an interesting technique to enhance the performance of MOSFETs in integrated converters which could change the threshold voltage by applying appropriate voltage to body-to-source in a way that reduces the conduction and switching losses when the switches are ON, and improves the static power consumption when the switches are OFF. This approach meets both the design considerations of switching converters and the design limitations in LSI level. ABB has two modes: during the operation of circuit using Forward Body Bias (FBB), the threshold voltage decreases and using Reverse Body Biasing (RBB), the threshold voltage increases. Therefore based on the status of the synchronous buck converter switches, the performance of the circuit could be enhanced adaptively.

In this article, an integrated synchronous buck converter is presented which uses a body biasing control circuit with the least possible

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number of transistors in order to enhance the performance of the converter MOSFETs in ON and OFF modes thus, increases the efficiency. The rest of this paper is organized as follows: In Section 2, ABB and OUD methods are discussed. In Section 3, a brief review of the previous works is performed. The proposed integrated synchronous buck converter is presented in Section 4. The results and discussion are evaluated in Section 5. Finally, the conclusions are presented in Section 6.

2. Body biasing and over and under driving techniques

OUD and body biasing methods can be used to improve the characteristics of the MOSFETs. Using these methods the features of the MOSFETs could be changed during their operation [26–30]. According to Eq. (1), by applying a voltage to body-source, the threshold voltage of the MOSFET can be controlled. When the NMOS (PMOS) transistor operates in ON mode, by applying Vss + Δv (Vdd-Δv) voltage to the body, the threshold voltage would be decreased. This method is called Forward Body Biasing (FBB). On the other hand, when NMOS (PMOS) transistor operates in OFF mode, by applying Vss-Δv (Vdd + Δv) voltage to the body, the threshold voltage would be increased; this method is called Reverse Body Biasing (RBB).

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\varphi_f + V_{SB}|} - \sqrt{|2\varphi_f|}\right) \quad (1)$$

where γ is the body-effect coefficient and φf is the Fermi potential.

OUD is another technique to enhance the performance of the converter switches, which is used to over driving the MOSFETs by applying Vdd + Δv (Vss-Δv) voltage to NMOS (PMOS) gate in ON mode, and under driving the MOSFETs by applying Vss-Δv (Vdd + Δv) voltage to NMOS (PMOS) gate in OFF mode [31]. In Section 5, the effect of OUD in MOSFETs performance in the buck converter will be discussed.

Using OUD and ABB methods while the MOSFETs are in ON mode and in the steady state, would increase the current flow ratio; and in the transient state, would enhance the switching speed. Also, in OFF mode would improve the static features of the MOSFETs and would decrease the static power consumption.

3. Previous works

With decreasing size in the advanced CMOS technology, and lowering the threshold voltage to less than 400 mV, the demand for designing high efficient power converters to regulate the 0.3–0.55 V output voltage with low output current (10 mA >) has increased [24].

So far, various types of step-down switching converters have been developed for low-voltage operations. The digital low-dropout (LDO) switching regulators have been suggested for near/sub-threshold logic circuit applications [24,31–34]. Using a particular mechanism, these converters prepare a condition for regulating the near/sub-threshold voltages. In this part, first a common method which provides the soft switching to reduce the losses of the SOC switching converters is being discussed. Then the applications of body biasing to enhance the performance of the converter in the related recent works is investigated.

In order to achieve a proper current flow, the width of the power MOSFETs in the synchronous buck converter should be wide enough, which results in a large capacitor (C_M) in the node that two MOSFETs are connected to each other (Fig. 1). In [1–3], the dead-times before the conduction of each MOSFET is determined, in order to provide ZVS conditions at turn ON for Mp and Mn by charging/discharging of V_M node capacitor through the buck filter inductor. To realize this condition, the converter should be designed at CCM/DCM boundary condition and the inductor peak current would twice the full load current. This method has some drawbacks. When the inductor current becomes negative, the required charge of C_M is supplied by C_f filter capacitor which causes ripple in the output voltage. Therefore, the output capacitor should be increased in order to reduce the output ripple. This would also cause additional power losses in the inductor resistance [1]. In this method, the effective duty cycle decreases and it is not possible to use it in CCM mode.

In [24] the FBB technique is used to control the buck converter. In the control circuit, a zero-crossing detector (ZCD) is used for sensing the V_M node voltage to detect a reduction in inductor current and changes the converter operating mode from CCM to DCM. This ZCD consists of a common source differential input amplifier in which with decreasing the threshold voltage of the amplifier MOSFETs via FBB, the amplifier head room voltage would reduce and makes it possible to sense lower voltages. Although this method has improved the converter functionality, however it has no effect on the efficiency enhancement.

In [25], a fix voltage is applied to the body of the PMOS power transistor via FBB which has improved the efficiency up to 1%. Applying FBB as a non-adaptive technique, reduces the transistor threshold voltage in both ON and OFF modes. Although this can decrease the MOSFET turn ON time, but it increases the turn OFF time. Consequently, the switching losses during the turn OFF time would increase. On the other hand, applying FBB to PMOS during OFF mode causes an increase in the leakage currents and consequently increases the static power consumption. In this work, the body voltage of NMOS power transistor is fixed and connected to ground.

In [35], a single-inductor dual-output DC-DC buck convertor is suggested which has used body biasing technique to decrease the resistance of the ON mode in the load-selecting transistors in which a complex control circuit changes the applied voltage to the body of the transistors between two different voltages. This method only uses FBB to decrease the threshold voltage of two PMOS pass transistors which

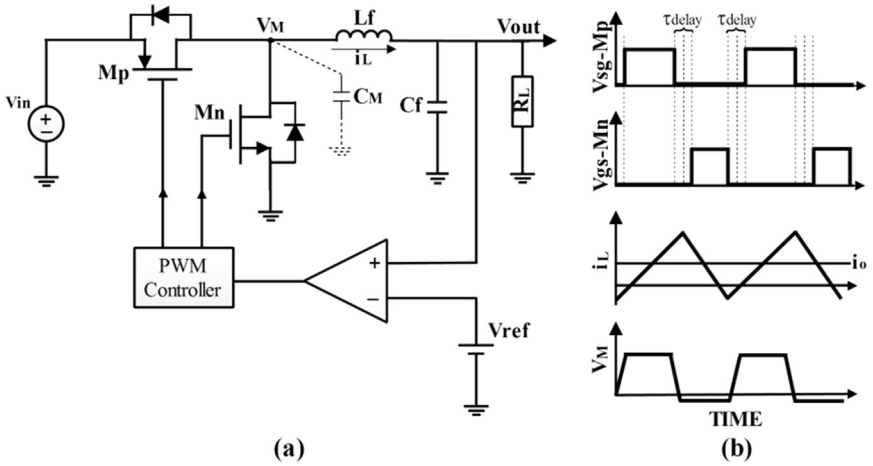

Fig. 1. ZVS synchronous DC-DC buck converter (a) circuit (b) waveforms.