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An accurate 1-V threshold voltage reference for ultra-low power applications

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ABSTRACT

An ultra-low power voltage reference circuit is presented, which is based on proportional (PTAT) and complementary (CTAT) to absolute temperature current generation and performs current-mode voltage reference with first-order temperature compensation. Thanks to the use of subthreshold CMOS transistors and an operational amplifier, the circuit achieves low sensitivity to power supply variations while providing low voltage capability. Measurements show that the proposed circuit provides a reference voltage of around 597 mV and correctly operates with a supply voltage ranging from 3.3 V to 1 V and temperature variations from −40 to 85 °C. The overall current consumption is below 1 μA, thus making it suitable for RF-powered and ultra-low power sensor network applications. The chip was fabricated in a standard 0.13-μm CMOS technology and occupies a core area as low as 0.02 mm^2.

1. Introduction

Low power and low voltage design techniques have become mandatory to meet the requirements of many integrated-circuit (IC) applications and also for technological reasons [1,2]. Indeed, low power design is essential in battery-operated systems to preserve operating time whereas in battery-less RF-powered systems guarantees fast start-up and better harvester sensitivity [3–6]. Moreover, low power and low voltage approach is of great importance in ICs with nanoscale technologies to avoid transistor breakdown and improve reliability.

By considering battery-less devices based on RF harvesting, the low power and low voltage design strategy involves all the functional blocks of the IC in both the analog and digital side, and mainly the power management unit (PMU) that greatly contributes to the overall power consumption. A key building block of a PMU is the voltage reference that sets the accuracy of the regulated power supply and determines its temperature behaviour.

Many approaches have been developed in the last decade to implement voltage references with low or even extremely low power consumption [7–17]. One of the most popular voltage references in CMOS technology for low voltage applications is shown in Fig. 1 [7]. It exploits a linear combination of proportional (i.e., PTAT) and complementary (i.e., CTAT) to absolute temperature currents to generate a reference voltage across resistance R_4. The circuit uses parasitic bipolar PNP transistors that have a poor performance in terms of current gain, β_F, and mainly suffers from the offset voltage due to the operational amplifier that greatly impacts accuracy.

To overcome the offset limitation, other types of current-mode voltage references are adopted [8,9]. However, they also employ parasitic bipolar transistors to perform PTAT and CTAT current generators.

There are also fully CMOS voltage references that make use of MOS transistors with different threshold voltages [10,11]. These circuits also avoid resistances, thus allowing to drastically reduce silicon area and power consumption. They can be designed with nano-ampere quiescent currents but exhibit a low accuracy, due to a high sensitivity to process variations, and require extra fabrication masks to implement different threshold voltages. Moreover, the reference voltage only depends on technology parameters and complex circuitry is needed to set a specific value.

In this paper, a fully standard CMOS threshold voltage reference is presented, which operates from 3.3 V down to a 1 V while exhibiting high accuracy against power supply variations. The circuit was designed for a battery-less transceiver based on RF energy harvesting [4,5]. It exploits MOS transistors operating in weak inversion for both PTAT and CTAT currents and an operational amplifier that improves accuracy of current matching and provides low voltage capability.

The paper is organized as follows. Section 2 deals with circuit description and design guidelines of the proposed voltage reference.

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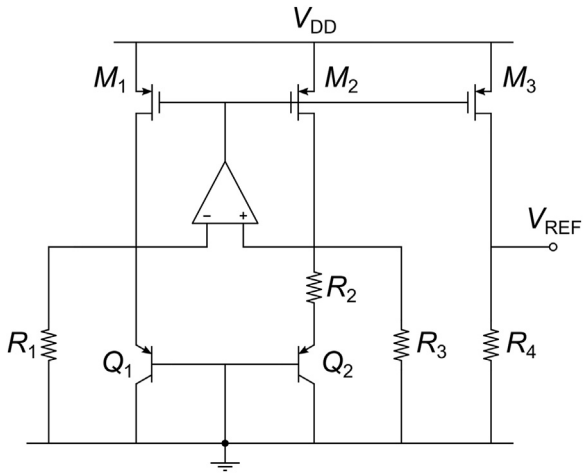

Fig. 1. Traditional low-voltage bandgap reference.

Section 3 summaries the experimental results. Finally, conclusions are drawn in Section 4.

2. Circuit description

The proposed voltage reference is based on the current-mode topology that was originally introduced by Yin et al. [8]. A simplified schematic of the proposed circuit is shown in Fig. 2. It uses PTAT and CTAT self-biased current generators, which are both derived from CMOS transistors M_1 and M_2, operating in subthreshold region, and resistances R_{PTAT} and R_{CTAT}, respectively. PTAT and CTAT currents are injected into resistance R_{OUT} and give the reference voltage, V_{REF}.

The main target of the proposed solution was achieving low voltage capability, low line sensitivity, and low small-signal power supply response (PSR), while providing operation in a wide range of supply voltages. This performance was obtained thanks to the use of subthreshold-biased MOS transistors and a transconductance operational amplifier (OPAMP). Indeed, the use of CMOS transistors in weak inversion instead of bipolar transistors has several advantages such as low gate-source voltage that reduces the minimum bias voltage and no gate current. Moreover, the operational amplifier improves accuracy of current matching besides guarantying low voltage capability and variable power supply.

The PTAT current generator is very similar to the conventional self-biased circuit. However, differently from the latter, the bipolar transistors are replaced by subthreshold-biased MOS transistors. The expression of the PTAT current is hence given by

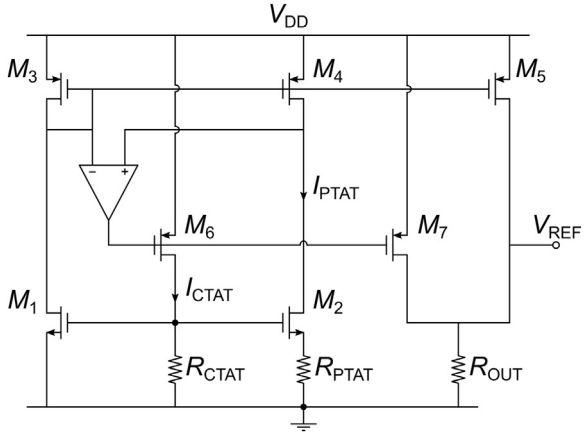

Fig. 2. Simplified schematic of the proposed threshold voltage reference.

$$I_{PTAT} = \frac{V_{PTAT}}{R_{PTAT}} = \frac{V_{GS_1} - V_{GS_2}}{R_{PTAT}} = \frac{mV_T \ln N}{R_{PTAT}} \tag{1}$$

where m and N are the subthreshold slope parameter and the ratio of the form factor of M_2 to the one of M_1, respectively, and V_T is the thermal voltage.

The use of subthreshold-biased MOS transistors in the CTAT current generator provides a negative temperature coefficient similar to the one of bipolar transistors [15]. However, CMOS transistors avoid the inaccuracy due to the contribution of base currents, which are not negligible since bipolar transistors of standard CMOS technologies suffer from a low β_F (i.e., typically lower than 20).

The expression of the CTAT current is [18].

$$I_{CTAT} = \frac{V_{GS_1}}{R_{CTAT}} = \frac{V_{th,0} + k_{t1}\left(\frac{T}{T_o} - 1\right) + mV_T \ln \frac{I_D}{\mu_n C_{OX} V_T^2 \left(\frac{W}{L}\right)_1}}{R_{CTAT}} \tag{2}$$

where $V_{th,0}$ is the threshold voltage at the nominal temperature T_0, k_{t1} is a temperature parameter of the threshold voltage, I_D is the drain current of M_1.

I_{PTAT} and I_{CTAT} currents are mirrored into R_{OUT} thanks to current mirrors M_{3-5} and M_{6-7}, respectively, providing reference voltage V_{REF} that is given by

$$V_{REF} = R_{OUT}(I_{PTAT} + I_{CTAT}) = \alpha V_T + \beta V_{GS_1} \tag{3}$$

where

$$\alpha = \frac{mR_{OUT} \ln N}{R_{PTAT}} \text{ and } \beta = \frac{R_{OUT}}{R_{CTAT}}.$$

By properly setting N and ratios R_{OUT}/R_{PTAT}, R_{OUT}/R_{CTAT}, cancellation of the temperature coefficient at a specific operating temperature can be achieved thus performing a first-order temperature compensation.

2.1. The operational amplifier

The operational amplifier in the proposed voltage reference is a key building block for performance parameters such as low sensitivity to power supply variations and low voltage capability, as mentioned before.

A complete schematic of the threshold voltage reference that includes the detailed topology of the OPAMP and the start-up circuit is shown in Fig. 3. The OPAMP is embedded in the PTAT and CTAT current generators. Indeed, it exploits transistors M_1 and M_2 and resistances R_{PTAT} and R_{CTAT}, which are key components of these generators. Although a two-stage OPAMP would be suitable to guarantee accuracy and low voltage capability, the differential stage (see Fig. 2) along with the voltage reference core and transistor M_6 inherently produce a three-stage amplifier. A reversed Nested-Miller compensation [19] is adopted for frequency stability. The OPAMP can be illustrated by the simplified block diagram in Fig. 4. The first stage is performed by the differential stage, M_{8-13} (see Fig. 3), and drives the second gain stage that is implemented by the cascode stage, $M_{6,1}$, $M_{6,2}$, loaded by R_{CTAT}. The third stage is made up of the conventional self-biased PTAT current generator, which is composed of transistors $M_{1-4,2}$ and resistance R_{PTAT}. The third stage includes two gain paths with opposite sign, whose signals are summed at the OPAMP inverting input terminal. The non-inverting gain path is composed of M_1 and low-voltage cascode current mirror $M_{3,1-4,2}$, whereas the inverting gain path is performed by M_2 and R_{PTAT}. The low-voltage cascode current mirror improves PTAT current accuracy against power supply variations while preserving low voltage capability.

The gains of the three stages of the open-loop amplifier in Fig. 4 can be expressed as