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# Variable strength keeper for high-speed and low-leakage carbon nanotube domino logic

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ABSTRACT

A new variable strength keeper technique is proposed in this paper for achieving robust, high-speed, and low-leakage dynamic logic gates with carbon nanotube transistors. The strength of keeper is dynamically adjusted depending on the logical state of dynamic node during input evaluation phase in a domino logic circuit. While providing similar noise immunity, the evaluation delay and power-delay product of proposed domino circuits are reduced by up to 13.33% and 13.84%, respectively, as compared to standard domino circuits in a 16 nm carbon nanotube transistor technology. Furthermore, the proposed domino circuits provide up to 77.98% savings in average leakage power consumption as compared to standard domino logic circuits in idle mode.

## 1. Introduction

Dynamic CMOS circuits display lower logical effort, switching threshold voltage, and parasitic capacitance characteristics as compared to static CMOS circuits [1]-[9,12]. Dynamic CMOS circuits thereby operate at a higher speed while occupying a smaller silicon area as compared to static CMOS circuits. Dynamic logic circuits are particularly well suited to implement wide OR functions. Unlike static CMOS circuits that suffer from a tall stack of PMOS transistors in the pull-up network and a high logical effort, logical effort is much lower and independent of the number of inputs in wide fan-in dynamic OR gates [1–9]. Subthreshold leakage currents of conventional silicon MOSFETs (Si-MOSFETs) are increased with technology scaling [10–12]. Robustness, speed performance, and power efficiency of dynamic CMOS circuits are degraded with increased leakage induced noise in scaled CMOS technologies. Degradation of electrical characteristics is particularly disturbing in high fan-in dynamic logic circuits with wide pull-down networks that produce large leakage currents.

Carbon nanotube MOSFETs (CN-MOSFETs) provide better scalability and performance with suppressed short-channel effects and higher carrier mobility as compared to conventional Si-MOSFETs [12–16]. Carbon is therefore a strong candidate to replace silicon as the fundamental building material of integrated circuits in the future [16].

In a standard domino (SD) logic gate, the logical state of dynamic node is preserved by a feedback keeper [1]. Keeper transistor acts against various noise sources, such as leakage, charge sharing, and crosstalk. The voltage state of dynamic node is thereby maintained in a noisy on-chip environment [1,2,22,23]. A *K*-input standard domino OR gate assuming a carbon nanotube transistor technology is shown in Fig. 1. The keeper is fully turned on at the beginning of evaluation phase. Provided that the pull-down transistor network of a domino logic gate is activated, the p-channel keeper and n-channel transistors in the pull-down network compete to determine the logical state of dynamic node. The keeper current that opposes the discharging of dynamic node (when the pulldown network is activated) is called contention current.

Higher conductivity of p-channel keeper transistor is desirable for achieving enhanced noise immunity in domino logic circuits. A stronger keeper transistor however produces higher contention current, thereby increasing the evaluation delay and power consumption. While moving along a carbon nanotube, electrons and holes display near ballistic transport with similar mobilities [12–16]. N-channel and p-channel CN-MOSFETs with identical physical dimensions therefore produce similar active currents in a carbon nanotube transistor technology [12]. Even a minimum-sized keeper transistor may have similar strength as compared to the pull-down network of a CN-MOSFET domino logic circuit. To increase speed performance and power efficiency, a keeper transistor that is weaker than a minimum sized transistor may be required in dynamic CMOS circuits with carbon nanotube transistors. A weak

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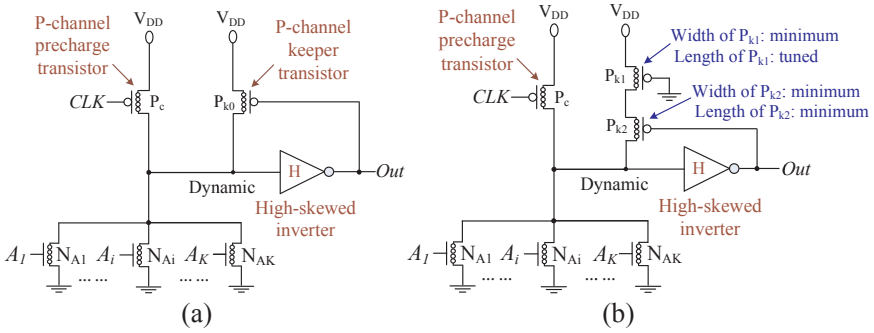


**Fig. 1.** K-input standard domino (SD) OR gates assuming a CN-MOSFET technology. (a) A stronger keeper transistor is desirable for wider noise margin. (b) A weaker keeper transistor is desirable for higher evaluation speed and lower power consumption.

keeper can be designed by connecting two transistors ($P_{k1}$ and $P_{k2}$) in series [12] as shown in Fig. 1(b). To achieve sufficiently high evaluation speed, however, the channel length of $P_{k1}$ needs to be significantly increased, thereby increasing the area of the dynamic logic gate with the carbon nanotube transistor technology. Furthermore, a smaller (weaker) keeper may not be able to provide sufficient noise immunity for reliable operation in the noisy environment of complex gigascale systems-on-chip. Leakage induced noise is particularly critical in dynamic logic gates with a high number (such as 8-inputs or more) of inputs and parallel pull-down leakage current paths. Achieving a satisfactory tradeoff between speed/power consumption and noise immunity is an important challenge in high-speed domino logic circuits with carbon nanotube transistors.

In this paper, a new variable strength keeper technique is proposed for robust, high-speed, and low-leakage wide fan-in dynamic logic gates with carbon nanotube transistors. The paper is organized as follows. The profiles of high-performance complementary CN-MOSFETs with 16 nm channel length that are used for designing domino logic circuits in this study are introduced in Section 2. The previously published keeper design techniques that are intended for the conventional silicon transistor technology are reviewed in Section 3. The proposed variable strength keeper technique specifically targeting carbon-based high-speed digital electronics is described in Section 4. The performances of wide fan-in dynamic OR gates with the proposed and previously published keeper circuit techniques are characterized and compared in Section 5. Finally, some conclusions are offered in Section 6.

## 2. 16nm carbon nanotube transistor technology

The physical parameters of CN-MOSFETs that are used in this study are presented in this section assuming a 16 nm CMOS technology. The study is based on the Stanford University CN-MOSFET HSPICE compact model [17]. Due to high switching activity factor ($\alpha$), power consumption of dynamic CMOS circuits tends to be high [2,12]. Dynamic CMOS circuits are therefore typically located at or near the hot-spots in microprocessors [12]. Die temperature is assumed to be 90 °C (a typical hot-spot temperature in current multi-core high-performance microprocessors [12–15,18]) in this study. Channel lengths of all the transistors are 16 nm ($L_g$ = 16 nm) in this study. Power supply voltage ($V_{DD}$) is 0.7 V [12–15].

A dynamic CN-MOSFET inverter is illustrated in Fig. 2. The complete set of physical parameters of 16 nm CN-MOSFETs is presented in [13]. The carbon nanotubes (CNs) are heavily doped with donors (for n-channel) or acceptors (for p-channel) in the source and drain extension regions of a CN-MOSFET. The carbon nanotubes are undoped under the gate. Nanotube diameter ($d_{CN}$) and nanoarray pitch ($s$) determine the performance and area of a carbon nanotube transistor [12–15]. The optimum uniform carbon nanotube diameter and nanoarray pitch are 0.84 nm and 5.3 nm, respectively, in both n-channel and p-channel transistors for achieving high performance while maintaining

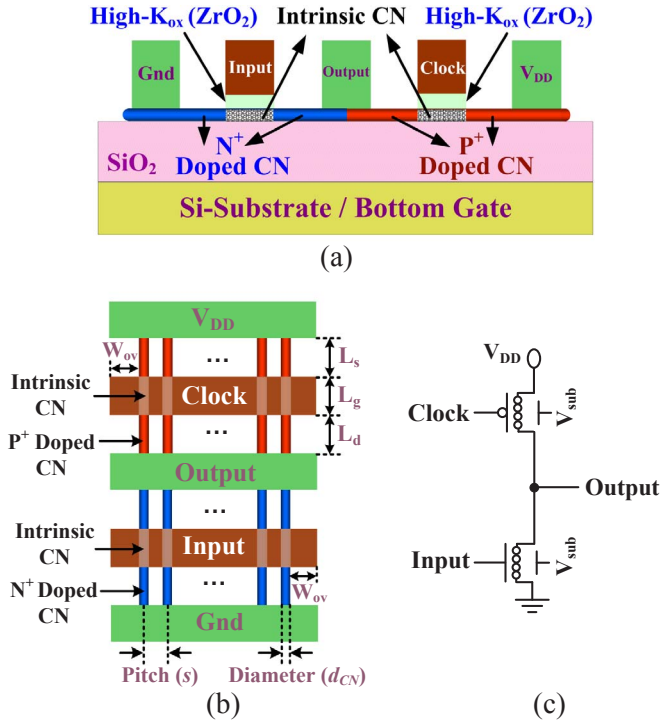


**Fig. 2.** A dynamic CMOS inverter with CN-MOSFETs. (a) Cross-sectional view. (b). Top view. (c) Schematic view. The substrate is shared by n-channel and p-channel CN-MOSFETs. The source/drain contact material: chromium/aurum (Cr/Au). The gate material: platinum/aurum (Pt/Au) [12]. A substrate bias voltage that is half of the power supply voltage ($V_{sub} = V_{DD}/2 = 0.35$ V) is employed for producing similar active currents with the n-channel and p-channel CN-MOSFETs [12].

high integration density as presented in [14,15].

The substrate acts as a second (bottom) gate below the thick oxide layer in a CN-MOSFET [12]-[15]. The substrate is shared by both n-channel and p-channel CN-MOSFETs in an integrated circuit. A substrate bias voltage that is half of the power supply voltage ($V_{sub} = V_{DD}/2 = 0.35$ V) is used for producing similar active currents with the n-channel and p-channel CN-MOSFETs in this study [12].

The strength of a CN-MOSFET is tuned by adjusting the number ($N$) of tubes that form the channel. The total area of a CN-MOSFET is determined by the physical gate width ($W_g$) [13]. $W_g$ is [13]

$$W_g(including\ \ overhangs) = s*(N-1) + d_{CN} + 2*W_{ov}, \quad (1)$$

where $s$ is the uniform array pitch, $N$ is the number of tubes in a CN-MOSFET, $d_{CN}$ is the uniform nanotube diameter, and $W_{ov}$ is the overhang width of the gate from the edge of CN array as shown in Fig. 2(b). $W_{ov}$ at each end is assumed to be 2λ (16 nm) [12–15,19] in this study. From Eq. (1), the physical gate width (including the overhangs) of a minimum sized CN-MOSFET with only one nanotube