Microelectronics Journal 62 (2017) 38–42

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# In-depth circuits edit analysis to reveal the implantation-related defect

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A R T I C L E I N F O

*Keywords:*
Circuit edit
Bipolar transistor
Implantation
Nanoprobing
Wright etch

A B S T R A C T

IC functional failure is always a challenge for failure analysis engineers since it needs test pattern to access the defect location and electrically trigger it. Dynamic failure analysis is the only way to be used to do this kind of analysis. But it's time consuming and complex to employ dynamic analysis, so the success rate is lower and cycle time is longer. Static failure analysis is impossible to apply on these kinds of analysis since the test pattern and design information is needed. However, in this paper, the application of advanced FIB circuit edit (CE) was employed to isolate the suspected function block, and make it accessible to the DC bias. With static FA analysis, the defect location was successfully localized. Nanoprobing was employed on the further electrical analysis, and abnormal electrical performance was successfully observed. Combined with the device physics analysis, the suspected process was identified. Further PFA Wright etch was applied to visualize the defect which was a soft failure of Bipolar Junction Transistor (BJT) device. Failure mechanism was built up to explain the electrical and physical phenomena successfully.

## 1. Introduction

Several lots with functional failure suffered from soft failures due to abnormal Band Gap voltage reference characteristics. The inline electrical monitoring structure showed no process parameter drift and wafer map pattern was inconsistent across the wafer and lot, but it was randomly failing in that functional block. Since Bandgap reference is a kind of common function block, the failing block can be easily identified through circuit analysis and GDS study.

Although it is easily to find the failed block in the die, dynamic analysis must be employed conventionally to do this kind of FA; it will has a longer cycle time; needs necessary test pattern and information for conventional FA.

For static FA, it is still impossible for us to access it and trigger it externally and electrically with the limited information and bias condition. That's why DC bias shows normal result on both bad and reference unit.

Since normal DC bias cannot work on this issue, an alternative approach by circuit edit was proposed to make FIB pad. The direct access on the structure by nanoprobing or microprobing will be available. Focus Ion beam (FIB) circuit edit, Atomic Force Probing (AFP) and Emission Microscopy (EMMI) analysis were adopted to analyze and narrow down the soft failure of defective BJT in this case study. Those FA techniques provide specific hints to understand the failure mechanism in terms of suspicious transistor.

Physical failure analysis was done by using by top-down delayering, and Wright etch method has also been used to delineate crystal defects. Since the Wright etch result was primarily determined by the abnormality in the implantation, the implantation related defect was visualized by using Wright etch method. Theoretically, the result was successfully linked with the device physics. Also, the problematic process was linked with physical defect. In the end of this paper, the electrical and physical investigations were successfully combined to find the failure root-cause.

In this paper, we present the combined electrical fault localization techniques incorporated with the conventional physical failure analysis (PFA) for implant related issues. The application of Wright etch is productive and effective in detecting abnormal implant profile issues.

## 2. Method and analysis

After analysis of suspicious bandgap circuit and GDS layout tracing, the investigation showed that the parasitic PNP-bipolar transistor with diode connection was applied in that kind of bandgap voltage reference as a complimentary to an absolute temperature (CTAT) structure [1]. That special bipolar transistor is the key-component within that function block. Furthermore that device occupies the major part of the block area. As shown in the Fig. 1, the yellow color is active area with a 5×5 bipolar transistors array.

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http://dx.doi.org/10.1016/j.mejo.2017.01.013
Received 21 July 2016; Received in revised form 23 January 2017; Accepted 23 January 2017
0026-2692/ © 2017 Published by Elsevier Ltd.

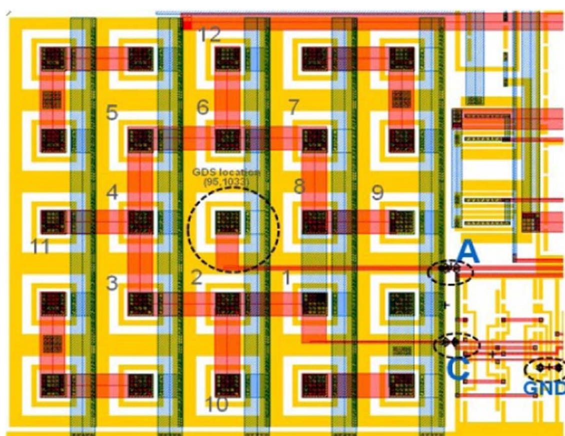


**Fig. 1.** Bandgap circuit layout, yellow color is Active, red color is metal connection. parallel connected bipolar 1–10 and the center bipolar in the circle are part of the bandgap circuit.

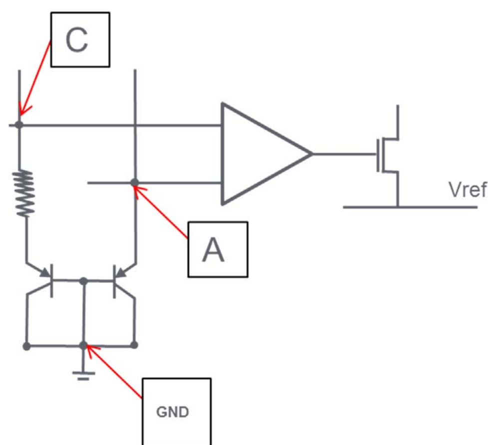


**Fig. 2.** schematic of the bandgap voltage reference, the square A, GND and C are FIB laid pad.

As shown in the Fig. 1, the parasitic vertical PNP bipolar transistors occupy the major part of the Bandgap circuit layout. Bipolar transistor 1–10 are parallel connected Based on our GDS analysis and circuit understanding, we come out with the principle schematic as shown in the Fig. 2. Since the circuit cannot be accessed externally by DC bias, the FIB circuit edit was conducted to get access to the local metal lines. As shown in the Fig. 2, three FIB-pads (pad-A, Pad-C and GND-Pad) were laid to connect the circuit within the highlighted node.

With those three FIB pad, the circuit can be accessed by DC bias to certain level. The combination of Vdd- and Vss-bondpad provide more flexibility to bias and trigger circuit by DC bias and static analysis.

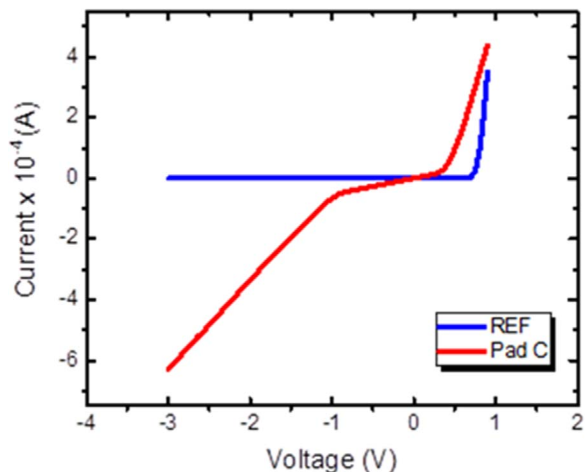


**Fig. 4.** IV curve of the pad C between bad and reference unit.

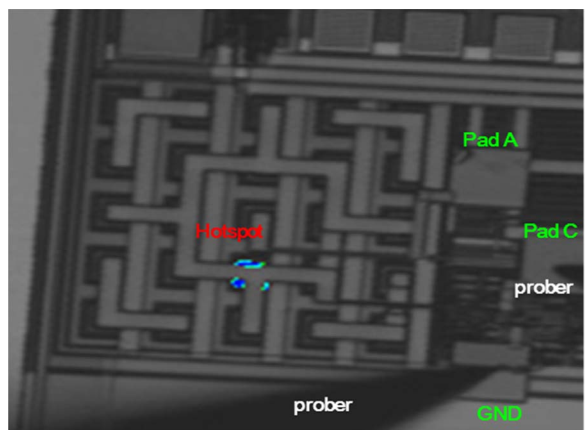


**Fig. 5.** EMMI analysis on the failed unit with FIB pad, probers were landed on Pad C and GND to do EMMI, hotspot observed in one of the Bipolar transistor, (scale bar removed due to company policy).

Based on the result, FIB circuit edit was done within fail-unit and reference-unit. The circuit edit is shown in the Fig. 3.

With those three FIB-pads, it was possible to get direct access to the major parts of the bandgap reference circuit, parasitic PNP transistors and operational amplifier.

DC performance of those pads was analyzed and compared with the reference unit. Surprisingly, different IV performance was observed on the FIB pad C between bad unit and reference unit, as shown in the Fig. 4. Although the structure was not isolated, the turn-on voltage of the bad unit is around 0.3 V which still trigger us to think about Schottky junction, because this value match with the Schottky junction

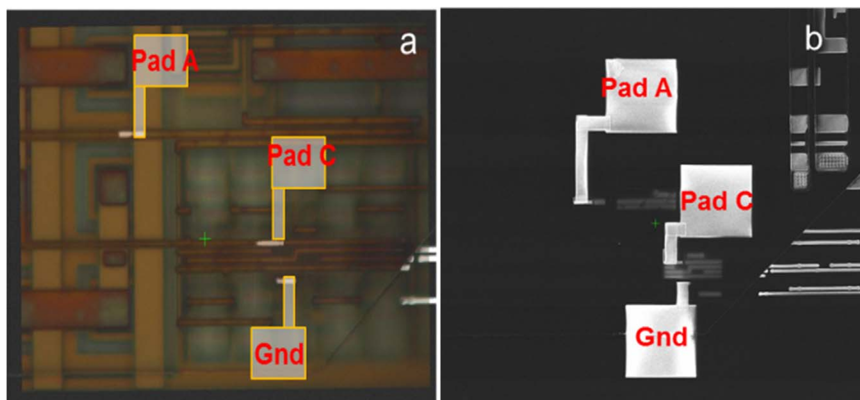


**Fig. 3.** image of the circuit edit. a, optical image; b, SEM image, (scale bar removed due to company policy).

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