CrossMark

Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI

J. Jeba Johannah[a],[*], Reeba Korah[b], Maria Kalavathy[c], Sivanandham[d]

[a] Department of ECE, St. Joseph's College of Engineering, Chennai 600119, India
[b] Department of ECE, Alliance College of Engineering and design, Bangalore 652106, India
[c] Department of CSE, St.Joseph's College of Engineering, Chennai 600119, India
[d] Department of ECE, Vellore Institute of Technology, Vellore, India

ARTICLE INFO

ABSTRACT

Scaling down of CMOS Technology reduces supply voltage which helps evade device botch caused by high electric fields in the conducting channel under the gate and gate oxide. Voltage scaling lessens circuit power consumption but increases delay of logic gates badly and the performance is degraded to a large extent in deep submicron CMOS VLSI circuits. In order to achieve good performance, the delay of logic gates has to be decreased. Circuits for trimming down of leakage power in sub-micron technologies also increase the dynamic power to a large extent. In this paper, a novel hybrid MTCMOS technique is proposed to reduce the enormous delay in gates due to sleep transistors; also, static power consumption is reduced without much affecting the dynamic power consumption of the circuit. For the 16-bit Ripple Carry Adder, the proposed technique can save up to 76.8% of static power consumption and 55.5% of dynamic power consumption also.

1. Introduction

In nano-scale technology, sub threshold leakage power upsurges exponentially with the lessening of supply voltage and threshold voltage. In several case-driven applications, standby leakage power becomes injurious on overall power dissipation. To provide high performance in dynamic mode and saving leakage power during static mode, various circuit level approaches are used. In CMOS logic, energy and charge conservation principle is used to derive the switching energy and power dissipation for static circuit. A load capacitance (C_L) is connected to the dc supply voltage V_{DD} through a pull-up network and to ground through a pull-down network. In the process of charging the output, the energy of $C_L V_{DD}^2$ is delivered to the load. The energy stored on the load capacitance charged to supply voltage is 1/2 $C_L V_{DD}^2$ and the other half must be dissipated in the pull-up network since energy cannot enter the ground rail. When the inputs are charged again, all energy is stored once again on the capacitance. This conventional logic represents maximum wastefulness, as the energy dissipation from delivery to removal of charge is in the form of heat.

This power dissipation can be reduced by involving many techniques. One such technique is adiabatic switching. But it requires pulsed power supply and the power supplies must be power efficient and must be able to recycle the power fed back to them. This technique cannot be

suitable when signal voltage is scaled down to minimize power dissipation or threshold voltage is reduced [1].

Another method to reduce power dissipation is charge recycling technique [2]. Many logic styles such as charge recycling differential logic, charge recycling bit line in SRAM and ROM are used to lessen power consumption and thereby the power dissipation in the preco-derlines is minimized. But for these techniques, the power supply needed is high and hence cannot be used for deep sub-micron processors [2].

Deep sub-micron CMOS circuits make use of process and circuit level techniques to reduce subthreshold power leakage. By varying dimensions of length, oxide thickness and junction depth, leakage power can be minimized at the process level. By controlling the voltages of source, drain, gate and substrate terminals, leakage power of transistors can be reduced at the circuit level. This paper analyzes various circuit level techniques to reduce sub-threshold leakage power in standby mode and to minimize total power consumption.

The best method that in practice to reduce leakage power is power gated CMOS circuits [3]. Power Gating also called as multi threshold CMOS is used to provide low leakage and high performance operation by using low threshold voltage transistors for logic cells implementation to accomplish high performance and high threshold voltage transistors for power gating switch implementation to decrease the

sub-threshold leakage current. The power gating switch can be implemented as a footer using single NMOS or as a header using PMOS or using both. This power gating transistor detaches logic cells from ground or V_{DD} rails or from both ground and V_{DD} rails to curtail inactive mode leakage power in the circuit. However power gating suffers from certain drawbacks [4]. One such drawback is that it needs revision in CMOS technology process to sustain both high threshold voltage device for sleep transistors and low threshold device for logic gates. Secondly, it lessens voltage swing and thereby the DC noise margin is reduced. Moreover, supply voltage scaling lessens the drive on all transistors. This results in the increase in the on-resistance of transistors and it is especially greater for power gating transistors since high threshold voltage devices are used. Also sizing of sleep transistor is a hard task and it requires much work. Consequently, larger sleep transistors are used and hence the area overhead of this approach rises. This paper proposes a new technique targeted at applications that demand low power and high performance. Power reduction is achieved by reducing V_{DD} and extra devices are used to improve performance and also to reduce leakage power.

2. Related work

Keshavarzi et al. [5] proposed dynamic threshold CMOS technique. This technique could be is applied only in partially depleted SOI devices. Seta et al. [6] suggested a technique called Reverse Body Bias [RBB] in the sleep-mode to reduce sub-threshold leakage. Keshavarzi et al. [5] said that RBB may lead to steep rise in junction leakage with biasing due to technology scaling. Mutoh et al. [7] recommended Multi threshold CMOS(MTCMOS). In MTCMOS circuits, both header and footer switches are used. Some modern circuits use either a header or a footer, to curtail the required area and the dynamic mode voltage drop. A header is PMOS device and a footer is NMOS device. A footer is mostly preferred as it needs less area for active mode since mobility of electrons is high. Only pull-up transistors are disturbed by a header and pull-down transistors are disturbed by a footer. High threshold voltage devices are used for both types of devices to reduce standby leakage and low threshold devices are used for logic gates. But this technique is not suitable for low supply voltages. Moreover, delay and area get increased in this method. Kuroda et al. [8] put forward a new technique named variable threshold CMOS technique. It is a type of body biasing design technique. But this technique cannot be engaged for deep sub-micron circuits. It needs a twin well or triple well technology as it requires a self- substrate bias circuit. Chen et al. [9] advised standby leakage control using transistor stacks. In this technique, leakage power depends on input vector pattern. Wei et al. [10] suggested dual threshold CMOS. Here finding out the critical path and assigning the threshold voltage differently to the critical path transistors is tedious. Kawaguchi et al. [11] presented a technique named super cutoff CMOS power gating technique. In this technique, an extra circuitry is essential to generate the required bias to apply to the footers. Tschanz et al. [12] offered a power gating technique with forward body biasing. But it functions with a drawback since it requires an additional circuitry. Shin et al. [13] projected a power gating technique called zigzag power gating. According to him, complicated power network is required for this technique. Roy et al. [14] recommended a power gating technique to maintain a voltage across the power gated logic to retain register state. Here, the area overhead increases. Mistry et al. [15] proposed sub clock power gating technique. This technique can be employed mainly in the active mode for low power energy constrained applications. Zhang et al. [16] suggested multi-mode power switches for static power reduction. In this technique, three transistors (one high threshold voltage V_t and two low threshold voltage V_t) are attached as footers to the main core to operate in four modes such as active mode, snore mode, dream mode and sleep mode. The advantage of this technique is that it can be applied to large cores. But it is deficient in many ways. First, it has much dynamic power consumption. Second, this technique

is only appropriate for static mode. Third, the power switches employed are digital and this technique cannot be applied for analog circuits.

This paper presents new and an effective power gating technique which has overcome the drawbacks of the above technique [16]. This proposed technique is suitable for both static mode and dynamic mode. This research paper combines power gating technique with reverse body biasing and also adds extra devices to enhance performance to reduce both dynamic and static power consumption.

3. Design considerations

Most of the power dissipation in CMOS circuits occurs due to logic transition which varies as the square of the supply voltage. Hence substantial savings in power dissipation may be extracted by operating with reduced supply voltage.

The power consumption of power gating circuitry is mainly consumed by the sleep transistor. It is important to make sure that the saved standby power using power gating technique should be greater than the power consumed by the circuit used for power gating. Coarse grain power gating and fine grain power gating are two main classifications in power gating [17]. In the first type, namely coarse grain power gating, a single sleep transistor is being shared by a large number of circuits. Here the area and power consumed by the sleep transistors are small. However if one of the circuits within this coarse grain domain is active, all the circuits which share the same sleep transistor cannot be set to sleep mode. Instead, in the second type namely, fine grain power gating, each circuit has an individual sleep transistor and hence if any one of the circuit is inactive, the same circuit can be set to sleep mode immediately. Hence the number of sleep transistors in fine grain power gating is much higher than that of coarse grain power gating. As the fine grain power gating is efficient to cut most of the standby and static power, such techniques are employed where standby or static power is a serious problem. The sleep transistor threshold voltage should be made large in order to reduce leakage current. Hence we use high threshold transistors as sleep transistors. Also care should be taken such that width of the power gating sleep transistor is chosen smaller than the total width of transistors in the pull-down circuit. However the area overhead for fine grain power gating approach increases as the number of sleep transistors are more compared to coarse grain power gating approach.

Moreover the size of the power gating transistors affects the logic circuit delay in the active mode. Also, the logic circuits are delayed as the voltage drop Δv occurs when current passes through the header/footer. The maximum current flowing through the power gating transistor namely header/footer concludes the voltage drop for a certain size of header/footer. The voltage drop across the header/footer should be proportional to logic circuit's total dynamic and active leakage current. Hence the header should be large enough in order to have a specified voltage drop for the current consumed by the logic circuit [13]. In general, the voltage drop Δv has two special effects: Firstly, the gate drive is diminished from supply voltage to $V_{DD} - \Delta v$ and the threshold voltage of the pull-down NMOS is increased due to body effect. These changes result in a decrease in the discharging current, which slows the output high to low transition. In practical designs, Δv need to be very small so that power gating does not introduce any significant extra delay. The delay in a CMOS gate is a function of V_{DD} and can be written as

$$Delay = \frac{C_L V_{DD}}{\beta (V_{DD} - V_T)^{\alpha}}$$

where C_L is the load capacitance, β is the gain factor, V_T is the threshold voltage and α is the velocity saturation index and α takes a value between 1 and 2 but usually closer to one. The corresponding delay when power gating technique is employed will be