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Analysis and design of cross-coupled charge pump for low power on chip applications

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ABSTRACT

This paper provides a comprehensive analysis of the operation of the CMOS charge pump, leading to a theoretical framework to aid low power designers in the optimization of its design in power constrained applications. An expression for the efficiency is derived as well as the optimum devices dimensions to maximize the latter for a given set of conditions (supply voltage, load current process parameters, etc.). The theory is verified through circuit simulations in Cadence environment using a CMOS 0.18 μm 6-metal layers technology.

1. Introduction

Small low power wearable system-on-chip (SoC) devices are the trend now for biomedical applications. These wearable devices consist of an integrated CMOS chip to process the signal, a printed circuit board (PCB) to mount the CMOS chip on, a sensor to extract the vital signal of interest and a battery. Most often, the battery is the bottleneck when it comes down to how small and light the system can be [1] and using as few batteries as possible is key to small size light weight systems. Small button cell batteries such as Zinc Air ones are typically used in wearable systems due to their small size and convenient round shape. These batteries usually have an operating voltage below 1.4 V [1], but some of the components in the system require higher voltages to operate. As a result, two batteries are needed which doubles the size and the weight of the wearable device. Alternatively a charge pump (CP) could be fabricated on chip and utilized to boost up the battery supply voltage to the required operating voltage. In this paper the operation of the CMOS cross-coupled CP is analyzed to provide a theoretical framework and design tips for low power applications, aiming to achieve the required voltage with the minimum power consumption, which is crucial in power constrained wearable devices.

2. Overview

Different variations of switched capacitor (SC) CP circuits are available in the literature, including the famous Dickson CP [2], and its CMOS implementation [3]. However, Dickson CP suffers from low efficiency due to the reverse charge sharing phenomena and the NMOS threshold voltage drop. The NCP1 and its improved version NCP2 [4] overcome this limitation. Another CP design based on the cross-coupled NMOS voltage doubler provides higher pumping efficiency compared to the Dickson or NCP-2 CPs, for a given set of conditions (supply voltage, load current and number of capacitors) [5,6] and it is the most popular for on chip applications [7]. Hence it is the one used in this work.

An extensive amount of work has been done on modeling and optimizing CP circuits [8–13]. The work reported in [8] provides a theoretical model of the transient behavior of two and three stages Dickson's CP. An area efficient optimized design methodology, based on this model, was also proposed. A further extension of this model to N-stages Dickson's CP was reported in [9]. Another design methodology to minimize the power consumption of Dickson's CP was introduced in [10]. This was based on optimizing the number of stages required to achieve a specific output voltage from a given input. An extension of the work done in [10] to other CP topologies was proposed in [11], where an analytical general model of the CP was introduced. This general model can be used to calculate and optimize the efficiency for different CP topologies by using some parameters that describe that specific topology. However to be able to use this model, it is first required to calculate a few parameters that are specific to the topology of the CP used. In [12], a design methodology to optimize the efficiency versus power density of a SC converter was proposed. This introduced gate drivers and level shifters design techniques to enable multiple topologies reconfiguration. It thus can be used to efficiently generate a range of output voltages. To further extend the optimization of CPs to a large number of stages (> 5), a new CP efficiency optimization method, based on matrix modeling of the pumping capacitors, was proposed in

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[13]. This was implemented as a CAD tool, making it suitable to analyze and optimize the efficiency of non-linear CPs topologies, such as Fibonacci and Exponential CPs, for a large number of stages without the need of complicated manual analysis. All the previously reported work is used either to optimize multiple stages CPs, or mainly for topologies different than the cross-coupled one. Cross-coupled CPs are, however, the most popular for on chip applications. Additionally, the design of clock drivers and the output MOS switches are not discussed. Moreover, miniature transducers that are used in novel wearable systems, such as microphones [14] and accelerometers [15], have an operating voltage range of 1.5 V–2.5 V with a current consumption range of tens to hundreds of micro-amps. Such components need a single stage CP to generate their supply voltage from 1 V–1.3 V button cell batteries. It is therefore useful for designers to have a complete and specific design methodology to optimize the efficiency of a single stage cross-coupled CP.

In this paper, the operation of the cross-coupled CP and different losses mechanisms within it are analyzed. Based on this analysis, design equations are developed. The derivation of design equations was carried out from first principles, in order to give designers an understanding of all the non-idealities in the CP as well as the factors that limit the CP's efficiency. The design equations subsequently lead to a complete design methodology that optimizes the efficiency of the single-stage CP. This design methodology includes all the design aspects of the CP, including the power losses due to the output PMOS switches and clock drivers. An expression for the optimum switch's dimensions, to minimize its losses, is also derived. In addition, a design procedure to reduce the power losses in the clock drivers is presented which leads to design recommendations for the clock generator, in order to optimize its power consumption as well.

The design methodology proposed in this paper can be used to make an educated decision on the choice of different design parameters in the CP to optimize its efficiency. The simulator is then used for verifying and slight tuning, if necessary. The rest of the paper is organized as follows: Section 3 analyzes the CP circuit operation and the effect of parasitic capacitances on its output voltage. Expressions for the average output voltage and ripple, while taking parasitics into account are then derived. Section 4 discusses the different power losses mechanisms within the CP. In Section 5 an expression for the efficiency is given. Based on that, an expression for the optimum output voltage for maximum efficiency is obtained. In Section 6, simulations are performed on the circuit in order to verify the theory and the design methodology. Section 7 summarizes the conclusions of the work.

3. Circuit architecture and analysis

The circuit diagram of the cross-coupled CP is shown in Fig. 1 [16] and its timing diagram in Fig. 2. The circuit is perfectly symmetrical and components all have the same design parameters. *CLK* and $\overline{CLK}$ are

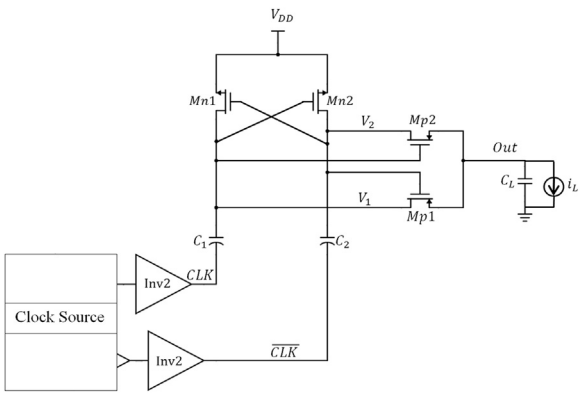

Fig. 1. Schematic of the cross-coupled CP with its pumping clock source.

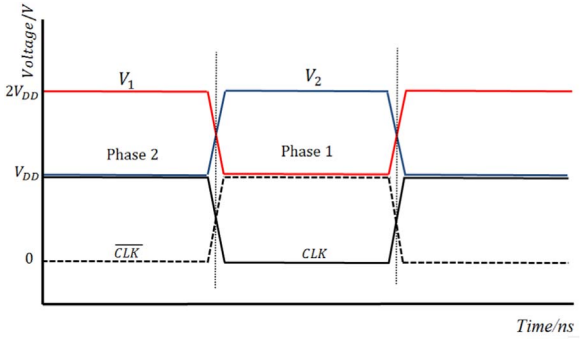

Fig. 2. Timing diagram of the cross-coupled CP showing the complementary clocks and the voltage swing at nodes V_1 and V_2.

two complementary clocks with an amplitude of V_{DD}. Define phase1 as when *CLK* is low and $\overline{CLK}$ is high, and phase 2 is the opposite. The circuit principle of operation in steady state is as follows: during phase 2 nodes V_1 and V_2 are at $2V_{DD}$ and V_{DD} respectively. *Mp1* is ON and *Mp2* is OFF and the output is at $2V_{DD}$. When the circuit enters phase1, *CLK* goes low and $\overline{CLK}$ goes high. Node V_1 is discharged to V_{DD} turning *Mn2* OFF and node V_2 is boosted to $2V_{DD}$ turning *Mn1* ON. This sequence of event turns *Mp2* ON and *Mp1* OFF, thus the output is at 2 V_{DD}. In phase 2 the roles of *Mn1* and *Mn2* are swapped, as well as the role of *Mp1* and M*p2*, and thus the output sees a constant voltage of 2 V_{DD}.

Assume in a first instance that there is no load and no parasitics. In phase2 *Mn2* is turned ON and node V_2 is at V_{DD}. The charge stored in C_2 during phase 2 is:

$$Q_{ph2} = C_2 \times V_{DD} \tag{1}$$

When the circuit enters phase 1*CLK* goes low turning *Mn2* OFF. As $\overline{CLK}$ goes to V_{DD}, the charge stored in C_2 must be conserved as there is nowhere for the current/charge to flow out (because *Mn2* are *Mp2* are still OFF and there are no parasitics connected to node V_2). Thus the voltage at the top plate of C_2 is boosted up to 2 V_{DD}.

If parasitic capacitances at node V_2 are taken into account (coming from the top plate ofC_2, gate of *Mp*, *Mn1* and drains of *Mp*, *Mn2*) then some charge must flow to these parasitics in order to raise their voltage above V_{DD}. As *Mn2* and *Mp2* are OFF, this charge comes from C_2 which results in a charge loss and voltage reduction, as shown in Fig. 3.

The reduction in voltage (V_{lost}) and the current that flows to the parasitics can be represented as follows:

$$V_{lost} = \frac{Q_{lost}}{C_2} \tag{2}$$

$$i_p = C_p \frac{dV_2}{dt} \tag{3}$$

where i_p is the current that flows from C_2 to C_p in order to charge it up and dV_2/dt is the rate of change of voltage at node V_2. Assuming that $\overline{CLK}$ transitions from low-to-high in linear fashion, the voltage at node

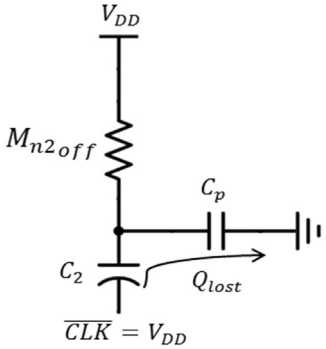

Fig. 3. Equivalent circuit explaining the lost charge due to parasitics in phase1.