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QLC NAND study and enhanced Gray coding methods for sixteen-level-based program algorithms

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ABSTRACT

After the development of TLC (Triple level cell) NAND, QLC (Quad level cell) technology will be one of the solutions for next generation NAND flash product. QLC (4 bits/cell) NAND's data levels are up to 16 levels which bring the narrower and tighter voltage ranges and worse performance. This paper studies QLC program and read mechanisms, and presents five types of program algorithms for writing data in QLC cells. Correspondingly, the enhanced Gray coding methods for data mapping based on these different program algorithms are researched. They will be beneficial to data reading. After simulating with changing cell voltages to generate the data errors in the QLC model, the paper presents four enhanced Gray codings to match 16 voltage levels for different program algorithms and read operations. This study will improve the efficiency and keep balance in system-level application for the data error correction of QLC 4 pages which are mapped in the same wordline (WL).

1. Introduction

In 1984, Dr. Fujio Masuoka of Toshiba Corp. invented Flash memory [1], after more than 30 years' development, NAND Flash technologies broke through many important technology nodes, innovated from 2D (two dimensional: scaling in X and Y dimension with planar photolithography [2]) to 3D (three dimensional: scaling in Z dimension for vertical layers with etching [3]), and from 2D 256Kb SLC (1 bit/cell) [4] to 2D MLC (2 bits/cell) [5], and to 3D MLC [6], and now to 768 Gb 3D TLC (3 bits/cell) [7]. It is amazing that the evolution of NAND technologies brought great changes in memory market and electronic industry.

By precisely controlling the threshold voltages (Vth), NAND cells can be designed to "n bits/cell": SLC NAND means 1 bit/cell (2 voltage levels, data = 1/0); MLC means 2bits/cell (4 voltage levels, data = 11/10/01/00); TLC means 3bits/cell (8 voltage levels, data = "111 ~ 000") and QLC means 4bits/cell (16 voltage levels, data = "1111 ~ 0000").

The cost per Gb of TLC is reduced because the bit number of cell is increased. But the notably increased density of TLC is not enough for the increasingly hungry requirement from huge storage market. The market requires new NAND products with lower cost/Gb and acceptable performance. 3D TLC technologies succeeded and properties are better than the planar NAND [8]. It encourages the study on QLC NAND as one of the good solutions in future memory market and industry. Especially, the client SSD which is mainly for personal laptops or computers, mobile devices and consumer electronics only need to use or store data for 2–5 years with a few hundreds of program/erase cycles, the QLC NAND will be one of the available devices.

This paper studies QLC NAND technology. Five program algorithms based on QLC 16 voltage levels are investigated. The read mechanism and the basic data mapping with "half-change" Gray coding are presented. Four enhanced Gray codings are reported according to the related program algorithms. The simulation results show that the enhanced Gray coding can reduce the maximum error bits of QLC 4 pages by at least 25%, and the rate of data errors can be balanced in QLC 4 pages.

2. NAND flash and data mapping

As shown in Fig. 1(a) is the basic architecture of NAND Flash cell which has two types in industry: Charge Trap (CT) MOSTET which is used by most of vendors (e.g. Samsung, Toshiba) and Floating Gate (FG) MOSTET which is used by Micron/Intel. Control Gate (CG) layer can be made of metal (e.g. Tungsten) or poly. Blocking Oxide (BOX) and Tunnel Oxide (TOX) layers can be made of SiO2 or Oxide-Nitride-Oxide (ONO). Storage layer can be made of SiN or FG. Fig. 1(b) is the 2D planar architecture of NAND chip which is mainly fabricated based on the photolithography technology. Bitline (BL) controls the bit address and wordline (WL) controls the page address. Bitline Select (BLS) and Soureline Select (SLS) control the turn-on or turn-off of the cells in the string. Fig. 1(c) is the 3D architecture of NAND chip which is fabricated

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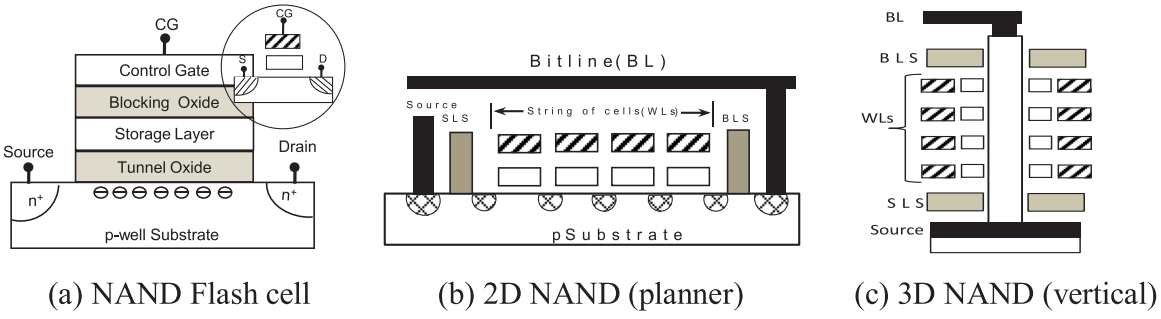


Fig. 1. NAND Cell and 2D/3D string architecture. (a) NAND Flash cell (b) 2D NAND (planner) (c) 3D NAND (vertical).

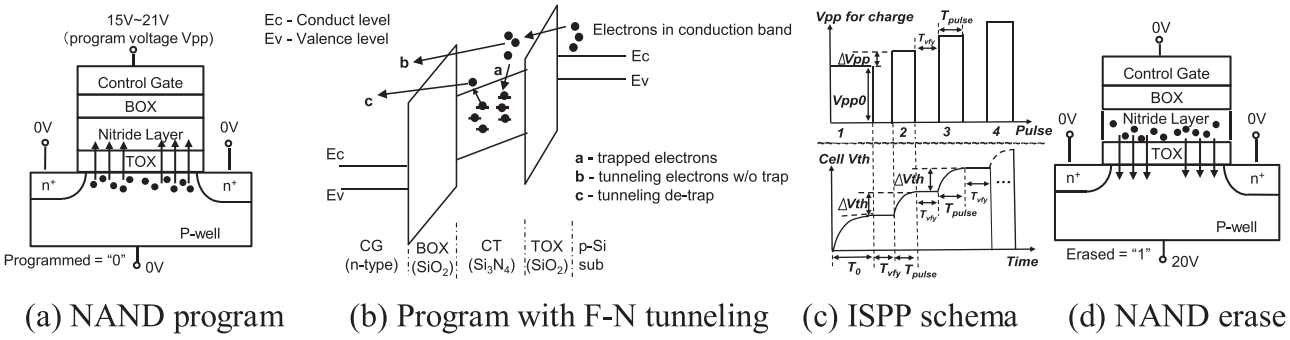
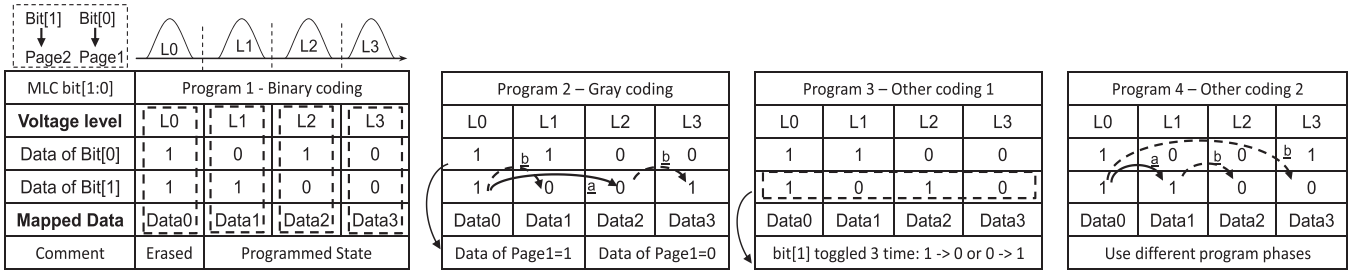


Fig. 2. NAND Flash programming mechanism and erase. (a) NAND program (b) Program with F-N tunneling (c) ISPP schema (d) NAND erase.

with multiple layers in vertical.

NAND Flash's program/read/erase operations are based on the accurate voltage control. Fig. 2 shows the program and erase operations of CT-based NAND. In Fig. 2(a), a high voltage bias (~20 V) is added to CG port and a lower voltage (~0 V) is added to the substrate, then the free electrons can be tunneled into the nitride layer through the TOX layer by Fowler-Nordheim (F-N) tunneling [9]. Fig. 2(b) shows the energy band for program operation. The electrons in conduction level are emitted and tunneled from the channel into the storage layer, some of them are deeply trapped in the storage layer (line a), and some are continually tunneled through BOX layer (line b), meanwhile, a few trapped electrons are thermally activated to be de-trapped through BOX dielectric layer (line c). When the trapped and de-trapped electrons are balanced after programming for time tPROG, charge is saturated and



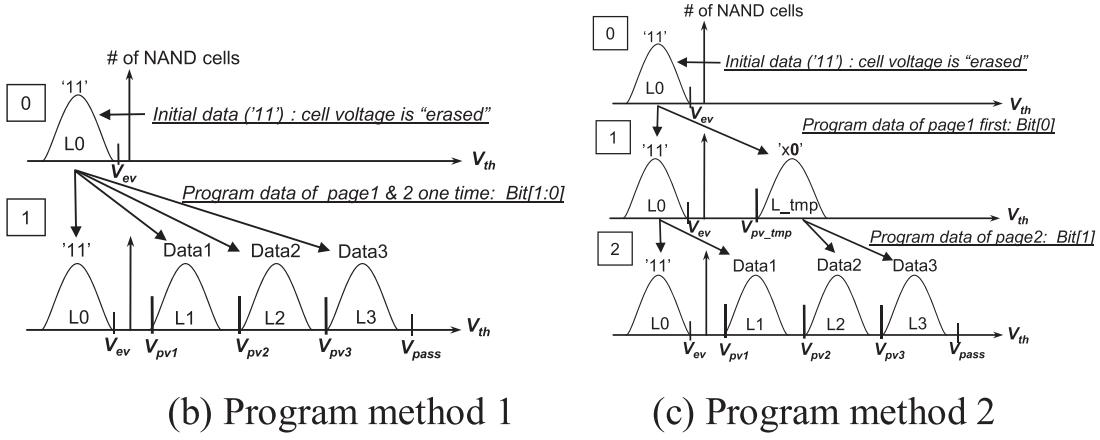


Fig. 3. Write data (program) in MLC NAND Flash cell. (a) 4 voltage levels and data mapping in MLC NAND. (b) Program method 1. (c) Program method 2.