Microelectronics Journal 66 (2017) 155–166

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Frequency compensation of three-stage operational amplifiers: Sensitivity and robustness analysis

Esmaeel Ranjbar, Mohammad Danaie*

Faculty of Electrical and Computer Engineering, Semnan University, Semnan, Iran

A R T I C L E I N F O

Keywords:
CMOS amplifiers
Compensation
Low-voltage circuits
Multistage opamps
Uncertainty

A B S T R A C T

Many different compensation techniques have been proposed in the literature for today's low-voltage multi-stage integrated opamps. Each of them tries to optimize their proposed designing procedure considering desired characteristics such as: slow rate, DC gain, power consumption and unity gain-bandwidth. However, the existence of uncertainty in the parameters of the opamps or the compensation elements can affect the optimality of their responses. Variation of the capacitive load of a compensated opamp is one of the probable sources of uncertainty. As a matter of fact, different compensation topologies do not exhibit equal sensitivity to the variation of capacitive loads. Therefore; the selection of a proper compensation technique is considered as an important step when designing an opamp. In this paper, the goal is to study the existing compensation techniques and their behavior in the presence of load uncertainty. It is our goal to present a guide which helps to choose the suitable compensation topology considering the level of uncertainty in capacitive loads. To achieve these goals the structures are first designed for equal performance metrics such as: gain bandwidth product, phase margin and settling time. Then the sensitivity of the different structures is evaluated. Thereby, the least sensitive structures can be chosen as good candidates for realization. Based on the knowledge of the authors, no such thorough analysis has ever been performed before.

1. Introduction

One of the most widely used integrated circuit components, is the operational amplifier (opamp). Opamps are vital elements in many analog and mixed (Analog-Digital) systems. Opamps with varying degrees of complexity, are widely used to accomplish various tasks such as generating DC biases, amplification, filtering, analog-to-digital and digital-to-analog convertertion, regulatoring etc. [1]. Uncertainty in elements' size is an important factor when designing opamps. Some obvious sources of uncertainties in opamps are: the approximations used in theoretical design, uncertainty in size of devices due to fabrication and litography error, temperature variation, non-linear effects, changes in the output load. Among the mentioned uncertainties, the uncertainty of load capacitors can sometimes be prevalent. Different opamp topologies behave differently when they are subjected to different types of uncertainties. Considering amplifier stability and obtaining proper frequency characteristics are important issues when designing opamps. The idea of compensation and stability in classical control theory is to place new poles and zeros in the open-loop system in order to satisfy different control criteria such as gain bandwidth (GBW), settling time (T_S) and phase margin (PM). Based on the type of compensation network, three-stage opamps can be divided into different structures. The main conventional methods used in these structures are feed-forward and feedback paths that are active or passive, such as: Miller compensation techniques [2–8], Nested Miller compensation using nulling resistor [9,10], Nested Miller compensation with current buffer [11,12], reverse Nested Miller compensation technique [13], compensation with active forward path [14,15], Nested Miller compensation with nested transconductance stage [16–22], damping-factor-control frequency compensation technique [23–25], frequency compensation technique by Single Miller capacitor [26].

According to the authors' studies, there has been no serious investigation about the impact of the load capacitance uncertainty on low voltage operational amplifier behavior. In some applications such as digital to analog converters variable capacitive loads can occur [27,28]. Some examples of circuits with variable or uncertain load capacitance are discussed in Section 3. When designing the opamps, variable capacitive load will act as an uncertainty source. It makes the optimal design difficult, because it affects the time and frequency characteristics of the system. In this paper, the effects of uncertain capacitive load on different aspects of frequency and time responses in low-voltage compensated three-stage opamps are reviewed. The results provide

* Correspondence to: Electrical Engineering Faculty, Semnan University, Semnan 35131-19111, Iran
E-mail address: danaie@semnan.ac.ir (M. Danaie).

http://dx.doi.org/10.1016/j.mejo.2017.06.010
Received 17 September 2016; Received in revised form 31 March 2017; Accepted 30 June 2017

guidance which helps the designer to choose the proper structure for its own application.

To design opamps there is a range of performance metrics to be taken into account [27–29]. Some of these metrics are: DC gain, output swing, slew rate, linearity, noise, offset voltage, stability and power comsuption. The design will be challenging if the designer considers all these parameters at once. Depending on the application of an operational amplifier, different parameters can be important and have to be taken into consideration. For example, one of the most important parameters of an operational amplifier used in switched-capacitors and analog-to-digital converters is settling time of step response. To obtain the optimal frequency parameters for low-voltage operational amplifier design, some techniques have been proposed in [1–4,30]. Moreover; some other design methods have been proposed to achieve optimal settling time in switched capacitor and analog-to-digital converters [1,31–37].

In order to be able to compare different compensation techniques, the first step is to design all the structures for required metrics such as phase margin, bandwidth and settling time. Then all the designed structures are evaluated based on sensitivity to capacitive loads and finally the less sensitive structure is selected. In order to do so, the rest of this paper is organized as follows: The analyses of the three-stage amplifiers are presented in Section 2. In Section 3, we introduce the design procedure and uncertainty analysis mechanism. The obtained results are presented in Section 4. Finally the last section is devoted to conclusions.

2. Compensation structures for three-stage low-voltage operational Amplifier

In this section, compensation methods for low-voltage operational amplifiers are reviewed. It is also described how operational amplifiers have evolved. In addition, advantages of each topology are investigated. Before explaining this section, the symbols used in this paper along with their explanations are introduced in Table 1.

Due to the nature of compensation structures, small signal transfer functions become extremely complex and cannot be analyzed easily. It makes the use of computers inevitable and numerical methods have to be employed. To simplify the transfer functions, some assumption are usually considered as follows:

- The gains of all stages are much greater than one (i.e. $g_{mi}R_{oi} >> 1$ and $g_{mL}R_L >> 1$).
- The loading and compensation capacitances are much larger than the lumped output parasitic capacitances of each stage (i.e. C_L, $C_m >> C_p$).
- Inter-stage coupling capacitances are negligible.

In the following paragraphs some of the most widely used compensation techniques for the three-stage low-voltage opamps are reviewed. In Fig. 1 the schematic diagram of the most famous compensation topologies are listed. These compensation techniques include:

2.1. Nested Miller Compensation (NMC)

A compensated opamp using NMC method has three-stages, including: inverting amplifier, non-inverting and inverting as the first, second and third stage respectively. As it is shown in Fig. 1-a, two compensation capacitors are used between gain stages in the NMC compensation. Fig. 2 is an example of a three-stage opamp using NMC implementation in which bias circuits have been excluded. The transfer function of NMC amplifier is as **(1)**. Hear after A_{dc} is used to represent the DC gain of the opamps.

$$A_{v(NMC)}(s) = \frac{A_{dc}\left(1 - s\frac{C_{m2}}{g_{mL}} - s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{\left(1 + s\frac{C_{m1}}{g_{m1}}A_{dc}\right)\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \tag{1}$$

2.2. Modified structure of NMC using nulling resistor (NMCNR)

According to small signal transfer function of NMC, this system has a right half plan (RHP) zero which adversely affects the frequency response of the amplifier. By adding a resistor in the compensation path, the right-plane zero problem can be addressed. Fig. 1-b shows the schematic diagram of NMCNR and **(2)** indicates its transfer function which is obtained after performing circuit analysis.

$$A_{v(NMCNR)}(s) = \frac{A_{dc}\left\{1 + s\left[C_{m1}R_m + C_{m2}(R_m - \frac{1}{g_{mL}})\right] + s^2\frac{C_{m1}C_{m2}(g_{m3}R_m - 1)}{g_{m2}g_{m3}}\right\}}{\left(1 + s\frac{C_{m1}}{g_{m1}}A_{dc}\right)\left[1 + s\frac{C_{m2}(g_{m3} - g_{m2})}{g_{m2}g_{m3}} + s^2\frac{(1 - g_{m2}R_m)C_LC_{m2}}{g_{m2}g_{m3}}\right]} \tag{2}$$

2.3. Multipath Nested Miller Compensation (MNMC)

For the compensation structures NMC and NMCNR due to the RHP zero, GBW is low. To move one of the RHP zeros to the left and achieve pole-zero cancelation, a transconductance stage is added to structure of NMC and in accordance with Fig. 1-c a schematic diagram for MNMC is produced. The small signal transfer function of MNMC is in according to **(3)**.

$$A_{v(MNMC)}(s) = \frac{A_{dc}(1 + s\frac{C_{m2}g_{mf1}}{g_{m1}g_{m2}})}{\left(1 + s\frac{C_{m1}}{g_{m1}}A_{dc}\right)(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}})} \tag{3}$$

2.4. Nested Gm-C Compensation (NGCC)

In this method, MNMC structure has to compensate one of the RHP zeroes by adding a transconductance stage. So, we can compensate both RHP zeros by adding two transconductance stages and we have two poles-zero cancelations. This idea is illustrated in Fig. 1-d and is referred to as NGCC. Eq. (4) shows the small signal transfer function of NGCC.

Table 1
Notations definition.

C_{mi}	C_{pi}	g_{mL}	g_{mfi}	g_{mi}
Compensation capacitor	Lumped i-th stage output parasitic capacitor	Load stage transconductance	i-th stage feed-forward transconductance	i-th gain stage transconductance
C_a, R_a	R_L	R_m	R_{oi}	C_L
Serial RC impedance	Load resistance	Nulling resistance	Output resistance	Loading capacitor
PM	***GBW***	$A_v(s)$	V_{out}	V_{in}
Phase margin	Gain-bandwidth product	Small signal transformer function	Output voltage signal	Input voltage signal