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A low-power capacitor switching scheme with low common-mode voltage variation for successive approximation ADC

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ABSTRACT

In this paper, a new low-energy switching technique with low common-mode voltage variation is proposed for successive-approximation analog-to-digital converters (SA-ADCs). In the proposed scheme, not only the switching energy consumed within the first three comparisons is less than zero, but also other comparisons are made with the low-power monotonic method. Therefore, the switching energy of the capacitive array, including the consumed energy during the sampling phase, is reduced by 90.68% compared with the conventional counterpart. Moreover, since the variation of the input common-mode voltage of the employed comparator is only $0.125V_{ref}$, where V_{ref} is the reference voltage of the ADC, the required comparator's performance can be much more relaxed leading to more power saving. Post-layout simulation results of a 10-bit 1-MS/s SA-ADC in a 0.18-μm CMOS technology show a signal-to-noise-and-distortion ratio (SNDR) of 61 dB, a spurious-free dynamic range (SFDR) of 79.8 dB, and an effective number of 9.84 bits. The ADC consumes 35.3 μW with a 1.8-V supply and achieves a Figure-of-Merit (FoM) of 38.5 fJ/conversion-step.

1. Introduction

IN wireless sensor networks' nodes, which changing batteries is impractical or impossible, battery-less devices that harvest energy from the environment are required. Therefore, low-voltage operation with high-power efficiency is desirable for these applications [1]. Hence, successive approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in low-power wireless sensor networks due to their minimal active analog circuit requirements and low power consumption. In high-resolution SA-ADCs, the employed capacitive-array digital-to-analog converter (DAC) consumes a large portion of the entire power consumption and also the occupied silicon area. Therefore, several capacitive-array architectures and switching algorithms have been presented in the literature to reduce the power consumption and the total capacitor size of the employed capacitive DAC [2–6]. Compared with the conventional structure, monotonic switching technique [2] has achieved a 50% reduction in the total capacitor size and a 81.26% reduction in the switching power consumption. The switching techniques presented in Ref. [3–5], and [6] have lowered the total capacitor size by 75% and the power consumption by 86%, 96.89%, 98%, and 98.83%, respectively. Even though the structure presented in [6] reduces the switching energy by 98.83, the large variation of the common-mode voltage in the fully-differential capacitive DAC causes a large variation in the offset and the input capacitance of the comparator, degrading the linearity of the converter. Hence, in this paper, a novel switching technique is proposed by which the power consumed within the first three comparisons is less than zero. Moreover, the rest of the comparisons are carried out by the monotonic low-power technique. Therefore, with the proposed technique, not only the switching energy of the capacitive array, including the consumed energy during the sampling phase, is reduced by 90.68% compared with the conventional SA-ADC, but also the variation of the input common-mode voltage of the comparator is only $0.125V_{ref}$ where V_{ref} is the reference voltage of the ADC. This makes the performance of the required comparator much more relaxed, leading to more power saving.

The rest of this paper is organized as follows. Section 2 presents the proposed switching technique. In Section 3, the design considerations of the proposed SA-ADC are discussed. Section 4 shows the simulation results verifying the efficiency of the proposed structure. Finally, the paper is concluded in Section 5.

2. Proposed SA-ADC

The schematic and the capacitor switching sequence of the proposed SA-ADC which consists of DAC_p (the capacitive-array DAC connected to

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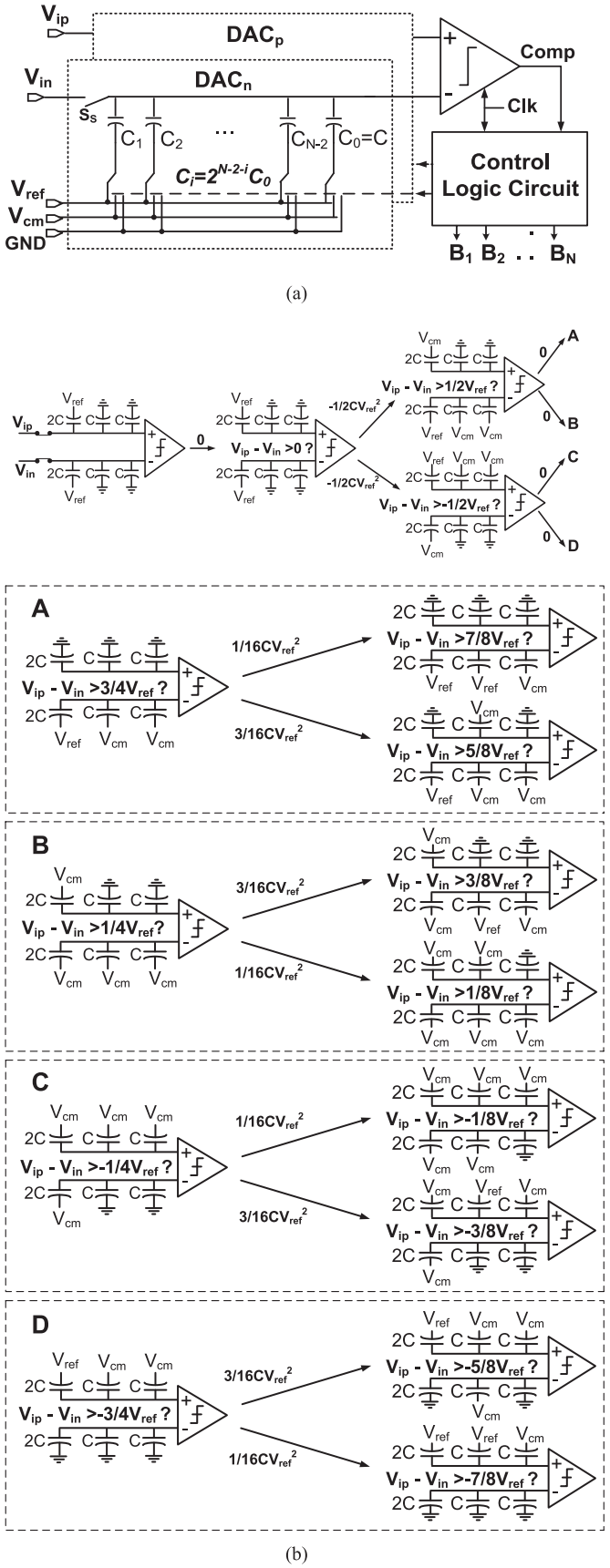

Fig. 1. (a) Schematic of the proposed SA-ADC. (b) The proposed capacitor switching technique in a 4-bit SA-ADC.

the comparator's positive input) and DAC_n (the capacitive-array DAC connected to the comparator's negative input) are shown in Fig. 1. The operation of the proposed structure is as follows. In the sampling phase, the capacitors of both DAC_p and DAC_n are set to *[1,0,0,...]*, i.e., the bottom plate of the largest capacitor (i.e., C_1) is connected to the reference voltage of V_{ref}, and the bottom plates of the other capacitors are connected to the ground. Simultaneously, the input analog signal is sampled on the top plates of all the capacitors. In the first cycle of the conversion phase, the sampling switches are opened and the first comparison is performed to determine the value of the most significant bit (i.e., B_1). Since there is no capacitor switching in the first cycle of the conversion phase, no current is drawn from neither V_{ref} nor $V_{cm}=0.5V_{ref}$. In the second cycle of the conversion phase, according to the result of the first comparison, the capacitors related to DAC_p (DAC_n) are switched to *[0.5,0,0,...]* (*[1,0.5,0.5,...]*) if $B_1=1$ or *[1,0.5,0.5,...]* (*[0.5,0,0,...]*) if $B_1=0$, and the second significant bit (i.e., B_2) will be determined. In other words, for $B_1=1(B_1=0)$, the largest capacitor of DAC_p (DAC_n) is connected to V_{cm} with the remaining capacitors connected to the ground. As for the capacitors of DAC_n (DAC_p), the largest capacitor (i.e., C_1) will remain unchanged and the other capacitors are connected to V_{cm}, as shown in Fig. 1(b). Therefore, the switching energy consumed during this cycle of conversion phase is

$$\begin{aligned} E &= C_1\left(\left(V_{cm}-\tfrac{1}{2}V_{cm}\right)-\left(V_{ref}-\tfrac{1}{2}V_{ref}\right)\right)V_{cm} \\ &\quad +C_1\left(\left(V_{ref}-\tfrac{3}{4}V_{ref}\right)-\left(V_{ref}-\tfrac{1}{2}V_{ref}\right)\right)V_{ref} \\ &\quad +(C_2+\ldots C_{N-2}+C_0)\left(\left(V_{cm}-\tfrac{3}{4}V_{ref}\right)-\left(0-\tfrac{1}{2}V_{ref}\right)\right)V_{cm} \\ &= -2^{N-5}C\,V_{ref}^2 \end{aligned} \quad (1)$$

where N is the resolution of the ADC, and C is the size of the unit capacitor. This negative energy implies that the capacitors give energy back to the reference voltage source (i.e., V_{ref}). In the third cycle of the comparison phase, for the case that $B_1=1$, only the bottom plate of the largest capacitor, i.e. C_1, of DAC_p (DAC_n) is switched to the ground (V_{cm}) if $B_2=1$ ($B_2=0$) and the other capacitors remain unchanged. Similarly, for the case that $B_1=0$, only the bottom plate of C_1 in the DAC_n (DAC_p) is switched to the ground (V_{cm}) if $B_2=1$ ($B_2=0$) and the other capacitors remain unchanged. It can be shown that this cycle of conversion also consumes no energy. For the remaining comparisons of the conversion phase, similar to the monotonic switching technique, for each cycle, based on the result of the previous comparison, the bottom plate of only one capacitor of either DAC_p or DAC_n is switched from V_{ref} to V_{cm} or from V_{cm} to the ground, as shown in Fig. 1(b).

In order to investigate the total switching energy consumption of the proposed structure during the conversion phase, it should be noted that the proposed scheme not only consumes no energy during the first and the third cycles of the conversion phase, but also consumes a negative energy during the second cycle. Moreover, for the other cycles, because of using the monotonic method, its energy consumption is small. Fig. 2 compares the switching energy consumption of the proposed scheme with some other works for different values of the output digital codes in a 10-bit SA-ADC. It can be observed that the proposed capacitor switching scheme consumes a $-16.13CV_{ref}^2$ average switching energy during the conversion phase. It should be noted that the negative switching energy is not non-physical, because by considering the consumed energy during the sampling phase, which overlooked in the previous works, a positive average switching will be achieved. In other words, considering the consumed energy during the sampling phase, the proposed method of switching achieves 90.63% reduction in the capacitor switching energy compared with its conventional counterpart, as will be discussed in Section 4. Finally, in order to study the variation of the common-mode voltage of the differential DAC in the proposed scheme, it is worth to note that, in the proposed structure, not only the common-mode voltage of the differential DAC remains constant during the first two cycles of the conversion phase,