



## Pre-distortion technique to improve linearity of low noise amplifier



Roya Jafarnejad<sup>a</sup>, Abumoslem Jannesari<sup>a,\*</sup>, Jafar Sobhi<sup>b</sup>

<sup>a</sup> Faculty of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran

<sup>b</sup> Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran

### ARTICLE INFO

#### Keywords:

Capacitive Cross Coupled (CCC)  
Common Gate Low Noise Amplifier (CG-LNA)  
High linear  
Pre-distortion  
Wideband  
Noise canceling

### ABSTRACT

A novel technique to improve the linearity of Low Noise Amplifier (LNA) based on pre-distortion in the input matching circuit is proposed. The linearization technique is applied to a Capacitive Cross Coupled Common Gate (CCC-CG) structure. An auxiliary transistor operating in weak inversion region is used to adjust the input matching circuit nonlinearity. It has been shown that the nonlinearity of input matching circuit can efficiently compensate the nonlinearity of transconductance ( $G_m$ ) of the amplifier, and improves the third Input Intercept Point (IIP3). Furthermore, the added transistor is used in a feedback path which provides a noise canceling scheme. Thus, linearity improvement is achieved in addition to low Noise Figure (NF). Post-layout simulation results in TSMC 0.18  $\mu\text{m}$  CMOS technology, show a gain of 18.55 dB with an upper  $-3$  dB frequency of 2.96 GHz, the minimum NF equals to 2.63 dB and IIP3 of 11 dBm, while consuming 2.77 mA from a 1.5 V supply.

### 1. Introduction

Multiband multistandard concepts have gained extensive research interest in modern wireless communication. Broadband transceivers support a wide set of communication standards (e.g., cellular communications at 900 and 1800 MHz, global positioning system at 1.2 and 1.5 GHz, LTE at 0.7–2.7 GHz, bluetooth at 2.4 GHz, and etc.) in a single device [1–3]. The Low Noise Amplifier (LNA) has an important role as the first building block of the receiver chain. Wideband LNAs compared with the multiple narrow-band LNAs can reduce the die area, the number of pins, cost and power consumption [1–3].

Such an LNA should achieve not only a high and flat gain with a low Noise Figure (NF) but also a wideband input impedance matching. Common Gate (CG) topology has been widely investigated as it provides wideband input matching, good linearity and stability. However, the main disadvantage of CG structure is its limited performance in terms of noise and gain [3]. Several methods such as multiple negative-positive feedback [2], noise canceling with the use of PMOS transistors and current reuse technique [3] and  $g_m$ -boosting technique [4] are reported to improve NF of CG LNA. These structures, however, have a degraded linearity.

A good linearity over a wide frequency range is a stringent requirement of wideband LNAs due to the presence of large number of in-band interferers and inter-modulations/cross-modulations produced by blockers at the LNA input. The second-order inter-modulation distortion (IMD2) and third-order inter-modulation distortion (IMD3)

of the LNA can considerably degrade the sensitivity of the overall receiver system in wideband receivers. Hence, in broadband applications, both second Input Intercept Point (IIP2) and third Input Intercept Point (IIP3) are important [5]. Nonetheless, most of the previously reported linearization techniques focused only on IIP3 improvement and targeted narrowband applications [6–8].

LNA linearization techniques should keep gain, noise figure and input matching while consuming minimum power and die area. Hence, it is a big design challenge and the most of linearization techniques for baseband circuits isn't applicable for LNA and requires innovative methods [9].

A well-known method for linearity improvement of LNA is the Derivative Superposition (DS) technique [6,10–15]. In the foregoing structure an auxiliary transistor operating in deep triode [6] or weak inversion [10] region is used to cancel out the 3rd order nonlinearity coefficient of the transconductance. The conventional DS method [6,10] which uses NMOS as the auxiliary transistor (Fig. 1a) usually worsen IIP2. However, Complementary DS employs an NMOS/PMOS pair to improve IIP3 without hurting IIP2 [11,12] (Fig. 1b). Although DS method works well in low frequency applications, the second order interaction at high frequencies limits its performance. The use of low impedance termination technique [11] solves this problem by setting the impedance of input or current source to low values at dc and  $2f_{RF}$  [10,13]. The technique is simple but on chip LC resonator consumes large chip area.

In DS method, the main and auxiliary transistors are placed in

\* Corresponding author.

E-mail addresses: [r.jafarnejad@modares.ac.ir](mailto:r.jafarnejad@modares.ac.ir) (R. Jafarnejad), [jannesari@modares.ac.ir](mailto:jannesari@modares.ac.ir) (A. Jannesari), [sobhi@tabrizu.ac.ir](mailto:sobhi@tabrizu.ac.ir) (J. Sobhi).

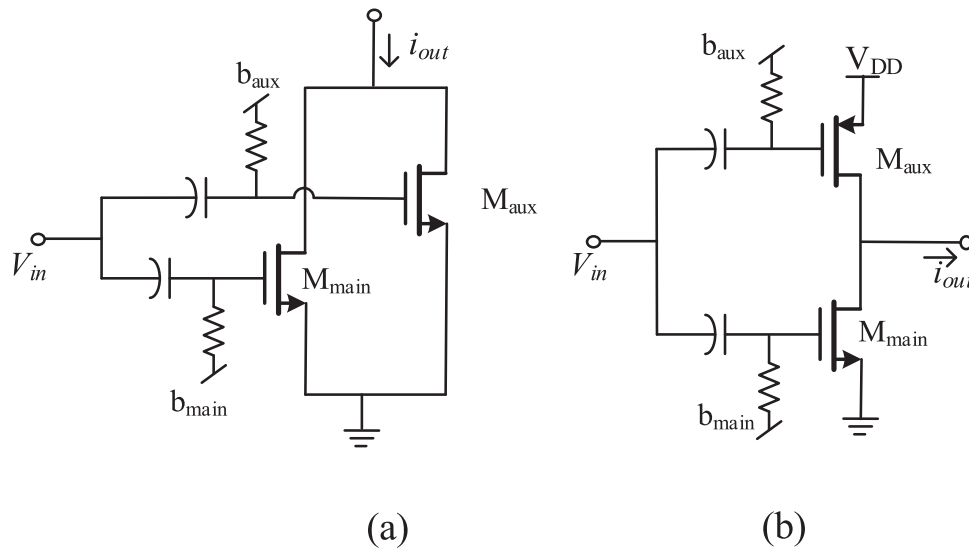


Fig. 1. Simplified schematic of derivative superposition method using (a) dual NMOS. (b) complementary NMOS/PMOS.

parallel with their gate connected together. A transistor operating in subthreshold region provides negligible drain noise. However, its gate noise is significant, since it is inversely proportional to the drain current. Therefore, the gate induced noise of the auxiliary transistor degrades the NF significantly [9,14]. Moreover, it is difficult to design a high gain, low NF with good input matching of the amplifier, specially over a wide band of frequency.

Noise canceling is another technique, where an auxiliary path is provided to cancel out the channel thermal noise and distortion of the matching transistor [5,16–19]. Fig. 2 shows two basic noise canceling structures including Common-Gate Common-Source (CG-CS) [16,17] and Shunt Feedback (SFB) based [18,19] structures. Since, the auxiliary path is composed of a transistor operating in saturation region, noise canceling technique is a good option for the wideband LNAs. However, it is hard to eliminate the distortion generated from the auxiliary amplifier and its limit its performance. In addition, these structures often require high power consumption.

In [8,20–24] a post distortion technique was used (Fig. 3) by adding NMOS [8,20–22] or PMOS [23,25] transistor at the output node to sink the 3rd order nonlinearity of the main transistor for IIP3 improvement. Authors in [20,21,23] have used an auxiliary transistor operating in strong inversion region, however in [8,22,25] a weak inversion transistor has used. Just like DS method using PMOS auxiliary transistor can improve both IIP2 and IIP3 [24], while NMOS transistor may impair IIP2. Post distortion method relaxes the design of main amplifier independent of auxiliary transistor for optimizing the input matching and reducing NF [25]. However, most techniques cause slight gain

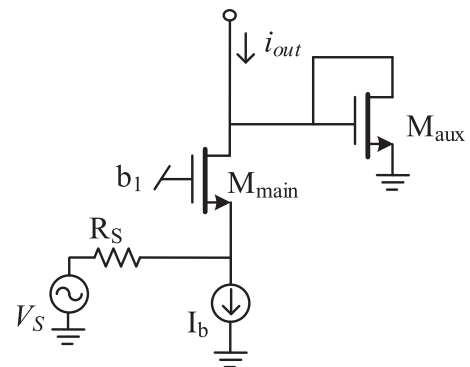


Fig. 3. Simplified schematic of post distortion method.

reduction and NF increment, due to fundamental current leakage through auxiliary transistor [20,21,23,24].

In most of the recently published techniques transconductance linearization is accomplished without any concern about the input matching network and its effects on the total circuit nonlinearity.

In this paper pre-distortion technique is proposed to enhance the linearity of low noise amplifier. A high linear wideband Capacitive Cross Coupled CG (CCC-CG) LNA is designed based on the proposed linearization technique. Mathematical analyses show that in the proposed structure linearity improvement is simultaneous with the NF reduction and gain enhancement, while keeping the desired input matching over the frequency band.

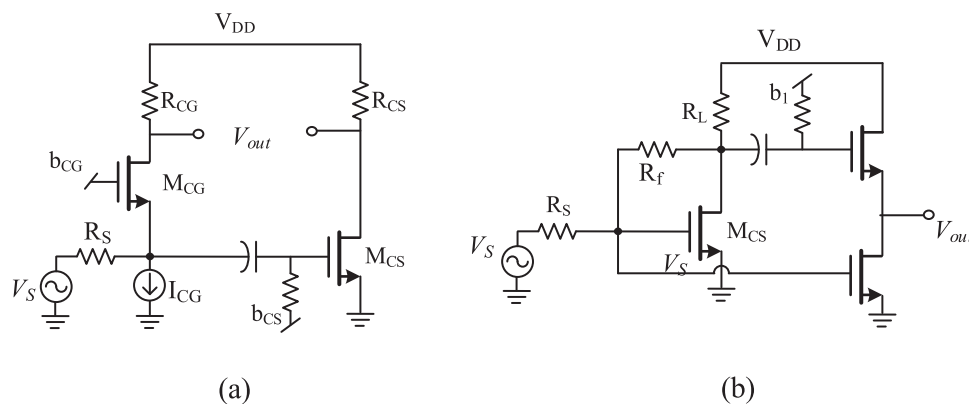


Fig. 2. Simplified schematic of noise canceling method using (a) CS-CG structure. (b) SFB based structure.

Download English Version:

<https://daneshyari.com/en/article/4971310>

Download Persian Version:

<https://daneshyari.com/article/4971310>

[Daneshyari.com](https://daneshyari.com)