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Self-directed channel memristor for high temperature operation

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ABSTRACT

Ion-conducting memristors comprised of the layered chalcogenide materials Ge_2Se_3/SnSe/Ag are described. The memristor, termed a self-directed channel (SDC) device, can be classified as a generic memristor and can tolerate continuous high temperature operation (at least 150 °C). Unlike other chalcogenide-based ion conducting device types, the SDC device does not require complicated fabrication steps, such as photodoping or thermal annealing, making these devices faster and more reliable to fabricate. Device pulsed response shows fast state switching in the 10^{-9} s range. Device cycling at both room temperature and 140 °C show write endurance of at least 1 billion.

1. Introduction

Memristors [1] have been studied intensely for the past several years due to their potential use in applications such as non-volatile memory [2], neuromorphic and bio-inspired computing [3–8], and threshold logic [9].

The type of memristor described in this work is an ion-conducting device (also referred to as an electrochemical metallization, ECM, device) which relies on Ag^+ movement into channels within the device active layer to change the device resistance. This memristor, referred to as a self-directed channel (SDC) device, uses a metal-catalyzed reaction within the device active layer to generate permanent conductive channels that contain Ag agglomeration sites. The amount of Ag within the channel determines the resistance of the device.

In this work, electrical properties of the layered memristor device are presented. These include the response of the device to a quasi-static DC IV sweep as a function of temperature and compliance current, frequency response to a sinusoidal input signal, write endurance, and pulsed response.

2. Device operation

Before describing the operation of the SDC memristor, it must be noted that this device should not be confused with another type of ion-conducting device which also uses Ag or Cu ions to change device resistance, referred to as the 'conductive bridge' device (often referred to as CBRAM and also as programmable metallization cell, PMC) [10]. Similarities between the SDC and CBRAM devices are that both typically use chalcogenide materials as the active layer such as As_xS_y [11], AgInSbTe [12], Ge_xSe_y, or Ge_xS_y [13,14] and both use an easily oxidizable metal, such as Cu or Ag, to change the device conductivity [2,10–17]. However, there are significant differences between the SDC device and CBRAM device. First, the CBRAM device changes resistance through a mechanism involving the formation and dissolution of a conductive filament between the top and bottom electrodes in response to a potential applied across the device [10]. Second, in the CBRAM device a Cu or Ag metal layer in contact with the chalcogenide active layer is the source of metal ions generated by an applied potential across the device. These ions migrate toward the more negative electrode under an applied potential, where they get reduced and build-up a metallic filament towards the positive electrode which eventually bridges the two electrodes and reduces the device resistance [10]. Reversing voltage polarities between the electrodes causes the conductive filament to disperse, thus increasing the device resistance. In the SDC device, the Cu or Ag metal layer cannot be adjacent to the chalcogenide active layer. Third, the largest difference between the SDC and CBRAM type of chalcogenide-based ion-conducting devices is that the CBRAM is typically fabricated using Se-rich or S-rich glasses by either depositing a ternary material (e.g. Ge-S-Ag) to a desired stoichiometry [16], or by photodoping and/or thermally annealing the Ag or Cu metal into the active amorphous material matrix [10,13,16,21–23]. To achieve the proper concentration of metal in the glass, precise control of the amount of metal included in the chalcogenide and the stoichiometry of the chalcogenide material is required. Both of these are challenging to achieve and are critical to the consistent operation of the CBRAM device [18–20]. In addition, the photodoping/annealing fabrication methods significantly reduce the maximum temperature exposure of the device during operation and fabrication. Two major factors that contribute to this are: 1) once the Ag or Cu has been added to the material, reduction in the glass transition temperature occurs and with exposure to higher temperatures this can result in crystallization of the glass, which damages device function-

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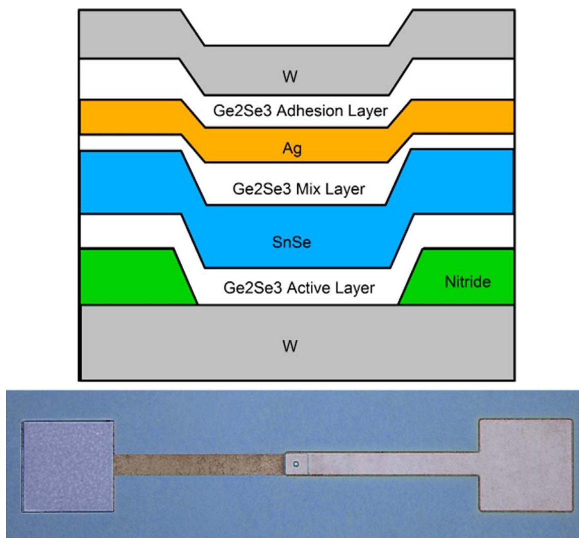

Fig. 1. Memristor device structure. Top: device layers. Bottom: fabricated device showing top electrode (right) and bottom electrode (left) bond pads for electrical probing. The layer thicknesses are not to scale relative to each other.

ality; and 2) the chalcogenides are prone to over saturation by diffusion of the metal layer into the active layer at higher temperatures.

In contrast to CBRAM, the SDC device, Fig. 1, uses a Ge-rich chalcogenide glass, Ge_2Se_3, and no photodoping or thermal annealing. Also, the SDC device is operational immediately after fabrication. The Ge_2Se_3 active layer is where device switching occurs; the key feature of this material is the presence of Ge-Ge homopolar bonds. The three layers consisting of Ge_2Se_3/Ag/Ge_2Se_3, directly below the top W electrode, mix together during deposition and jointly form the Ag-source layer. This Ag-source layer is not in direct contact with the active layer. This allows the device to have significantly higher processing and operating temperatures (above 250 °C and at least 150 °C, respectively) since Ag does not migrate into the active layer at high temperatures, and the active layer maintains a high glass transition temperature (~350 °C). These processing and operating temperatures are higher than most ion-conducting chalcogenide device types, including the S-based glasses (e.g. GeS) that need to be photodoped or thermally annealed. It is a combination of these factors that allow the SDC device to operate over a wide range of temperatures, including long-term continuous operation at 150 °C. The SnSe layer assists in the selective incorporation of Ag ions into the Ge_2Se_3 layer. This is done by incorporation of Sn ions during the first forming step of the device, likely near the regions of Ge-Ge bonding within the Ge_2Se_3 layer [24–28].

It should be noted that while the layered SDC device structure looks complicated due to the number of material layers, it is actually simpler and more reliable to fabricate than the CBRAM device. The entire deposition of the film layers, including the top electrode, is done in-situ in one processing step using a standard sputter tool. No extra time is required for photodoping or annealing, as is needed for the CBRAM device. Additionally, layer thicknesses are not critical; the active layer could be considered the only thickness sensitive layer, but it has a wide margin of acceptable variation, between 300 and 500 Å. Wafer-to-wafer consistency is therefore high, as across-wafer film thickness variation is not a factor. Because tight controls do not need to be in place for maintaining film thicknesses to tight tolerances, tool qualifications can be done less frequently and a production line could continue for longer periods without being out of specification. Because of this, wafer yields, in terms of number of functional devices per wafer, for the SDC devices are typically $> 90\%$.

In contrast, the CBRAM device depends critically on the amount of Ag incorporated into the device during photodoping/annealing. This means that the glass thickness and the Ag thickness need to be well-controlled as slight variations can cause the device to switch poorly (too little Ag) or to become saturated (too much Ag). The photodoping step also depends on good thickness control since the time of light exposure is linked to the amount of Ag incorporated into the device during processing. Consequently, the processes need to be frequently monitored and tools qualified more often. This translates to production down time and frequent poor yields. Additional complications of the CBRAM device fabrication include the device sensitivity to light exposure. As Ag can be photodoped into the device during light exposure, the wafers must be maintained in a dark environment until the risk of photodoping is removed.

In summary, five main factors differentiate the SDC device in terms of operation and fabrication:

1. The device can operate continuously at 150 °C without degradation.
2. No photodoping or thermal annealing is required, saving time, money, and handling risks.
3. The in-situ deposition of all device layers, including the top electrode, occurs with a standard sputter deposition tool in a single step.
4. Film thicknesses in the stack are not critical.
5. Cost is reduced due to a decrease in processing time, use of a single sputter deposition, reduction in qual/down time, and increased yield.

SDC devices are initially in a high resistance state (MΩ–GΩ range) following fabrication. The first time a device is operated after fabrication the device self-directed channel is formed during application of a positive potential to the top electrode. The potential required for this operation is the same as required during normal device operation. This first operation generates Sn ions from the SnSe layer and forces them into the active Ge_2Se_3 layer [24–26]. Theoretical calculations predict that these Sn ions facilitate the incorporation of Ag into the active layer at the Ge-Ge bonding sites [27]. This occurs through an energetically favorable process in which the electrons entering the active layer from the negative bottom electrode, concurrently with the formation of Sn ions from the SnSe layer, enable formation of a pair of self-trapped electrons in the Ge_2Se_3 active layer strongly localized around the Ge-Ge dimers present in this Ge-rich glass [28]. The result of this is that Sn ions facilitate an energetically favorable reaction of Ag substitution for Ge on the Ge-Ge bond. During this reaction, the glass network is distorted, creating an 'opening' near the Ge-Ge sites. The open regions provide good access for Ag^+ to the Ag-Ge site and become natural 'conductive channels' within the active layer for the movement of Ag^+ during device operation. This self-directed channel is a result of the natural glass structure and follows the location of the initial Ge-Ge dimers within the glass. Since Ag has a tendency to agglomerate with other Ag atoms, these sites may encourage Ag agglomeration within the glass. Thus, device resistance changes by adding or removing Ag from the agglomeration sites within this in-situ generated pathway. It is expected then that conduction could occur between clusters of Ag agglomeration sites [29,30]. This pathway does not therefore have to consist of conductive metallic filaments [31] spanning the two electrodes, as in the CBRAM device. It is simply a channel that has varying concentrations of Ag within it at these Ag agglomeration sites. The concentration of Ag at a given agglomeration site, and the distance between agglomeration sites dictates the device resistance. The resistance is tunable in the lower and higher directions by movement of Ag onto or away from these agglomeration sites through application of either a positive or negative potential, respectively, across the device.

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