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RF stability performance of SOI junctionless FinFET and impact of process variation

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ABSTRACT

In this paper we investigate the impact of process parameter variations such as temperature (T), channel doping concentration (N_D), Fin height (H_{fin}) and Fin width (W_{fin}) on Radio Frequency (RF) stability performance of 20 nm Silicon on Insulator Junctionless FinFET (SOI JLFinFET). The developed RF stability model provides relation between critical frequency (f_k) and small signal parameters which can be optimized for improved stability. Results shows as temperature increases (27–200 °C) cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) reduced by 12% and 8% respectively also stability factor (K) decreases by 20% at high frequency. Increasing N_D, H_{fin} and W_{fin} increases f_T and f_{max} but degrades stability performance. The result also provides optimized design guideline for operating SOI JLFinFET under RF range.

1. Introduction

Fabrication of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with metallurgical junction beyond sub 45 nm node has become extremely difficult due to the need of ultra-steep doping profiles [1]. C.-W. Lee et.al, A. Kranti et.al, and S. Gundapaneni et al. [2–4] have proposed junctionless transistor which don't have metallurgical junctions. Junctionless Transistor is a normally on device; it uses bulk conduction instead of surface conduction as like MOSFET hence to turn off the device we need to deplete the channel completely. In order to deplete the channel, a negative bias has to apply on gate terminal. By maintaining work function difference between metal gate and silicon, strong depletion in the channel can be created without applying negative gate voltage [5]. Multiple-gate Junctionless structures such as double gate and Trigate Junctionless transistors were proposed [6–8]. Among various multi-gate structures, triple gate structure is having better controllability over the channel and reduced SCEs.

The impact of variations on channel length, thin film thickness and random dopant fluctuation of Ground plane FinFET are presented [9,10]. Mohapatra et al., have studied the variations of Fin height and Fin width of SOI FinFET on RF Figure of Merits (FoM) such as cut-off frequency, output resistance, gate capacitance and intrinsic delay [11]. The effect of doping concentration and geometrical parameters such as Fin height and Fin width on Junctionless bulk FinFET were presented [12]. It was shown that channel doping variation will affect the threshold voltage and on-off ratio, similarly Fin height and Fin width variation will also affect the threshold voltage. Similarly the impact of body doping, body thickness, Fin height and channel length on dc parameters such as threshold voltage and Subthreshold Slope variation of SOI Junctionless FinFET were presented [13]. Many works were carried out to improve RF FoM such as maximum stable gain, maximum power gain, maximum oscillation frequency (f_{max}), and cutoff frequency (f_T) properties of multi-gate junctionless devices [14–17]. However, none of these literatures has studied RF stability which is one of the important selection components for the design of RF amplifiers. The RF stability performance of DG MOSFET, FinFET and Silicon Nanowire Transistor (SNWT) were presented [18–20]. In this paper, we comprehensively studied impact of process variation like doping concentration, temperature, along with geometrical parameters such as fin height and fin width on RF stability performance of SOI Junctionless FinFET. The organization of the paper is as follows. Section 2 provides the device structure and simulation setup in addition to device parameters. Section 3 presents process simulation and methodology and Section 4 presents RF Stability factor and modeling. Section 5 presents the results and discussions of this work. The proposed optimized structure with improved Radio Frequency stability is presented in Section 6. Finally, Section 7 concludes the work.

2. Process flow

In this study we have used Sentaurus process (Sprocess) for SOI JLFinFET design and Sentaurus device (Sdevice) for extracting its

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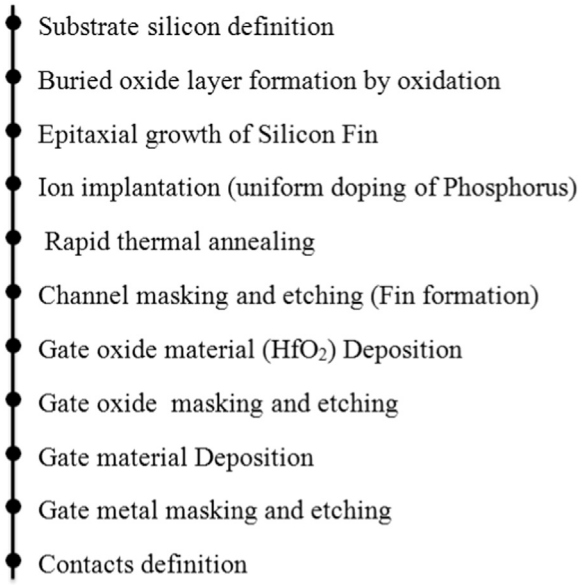

Fig. 1. Process Flow for SOI JLFinFET Structure creation in Sentaurus Process TCAD.

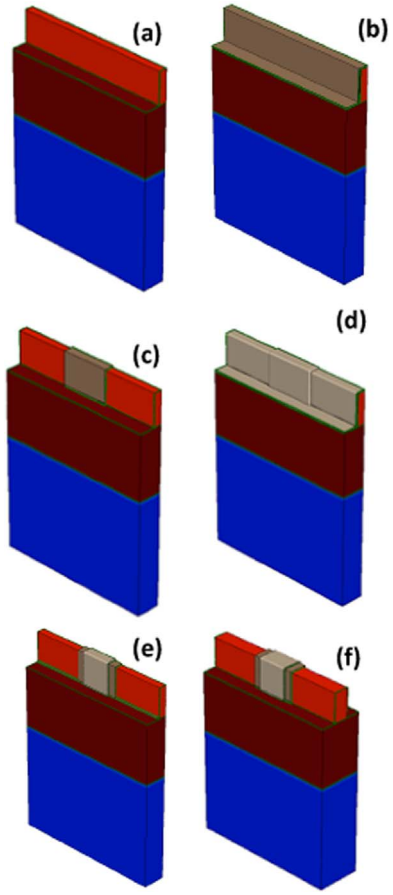

Fig. 2. (a-f) Schematic of SOI JLFinFET for processing steps listed in Fig. 1.

electrical characteristics. Fig. 1 shows the process steps involved in designing SOI JLFinFET. In Sentaurus process for symmetric structures there is a special feature available, in which users need to create one half of the structure another half will be created automatically by using reflect command. By specifying three dimensional (3D) coordinates substrate silicon is created with initial substrate concentration of Boron (1×10^{18} cm^{-3}). Then buried oxide layer is formed using oxidation by specifying temperature and time. For Fin formation silicon

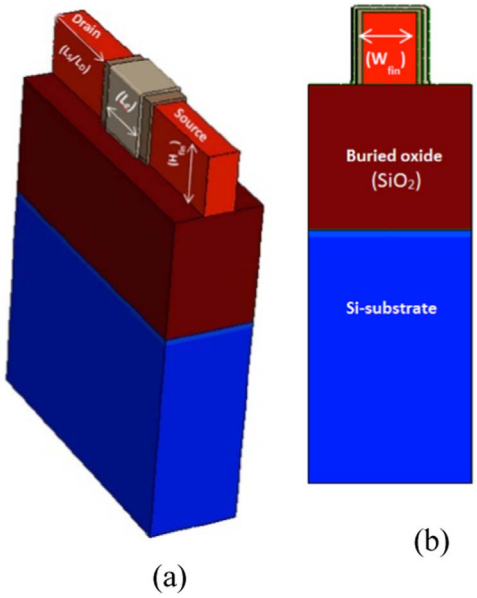

Fig. 3. (a) 3-D Schematic view of SOI JLFinFET (b) Cross-section view of SOI JLFinFET.

material is deposited then doped by ion implantation process by specifying species, energy and dose values. Here we have used Monte Carlo implantation process to achieve uniform doping across the Fin, followed by masking and etching process. Fig. 2(a) shows structure after buried oxide oxidation process and Fin formation. Then gate oxide layer (HfO_2) is created using deposition, followed by masking and etching process, the device structure after deposition and etching shown in Fig. 2(b) and (c) respectively. Similarly gate metal layer is created by metal deposition, masking and etching, device structure after deposition and etching shown in Fig. 2(d) and (e) respectively. By using transform reflect command, other half of the structure is created and the final device structure is shown in Fig. 2(f). Finally, source, drain and gate contacts have been made. After device creation using Sprocess the designed structure and temperature are given to Sdevice for electrical characteristics and parameter extraction. The detail of device simulation is presented in Section 3.

3. Device structure and simulation

Fig. 3 shows the 3D schematic view and cross section of SOI JLFinFET. The channel length chosen as 20 nm with source and drain lengths (L_S /L_D) of 40 nm as per ITRS [21]. We have used HfO_2 as gate oxide with the thickness of 0.9 nm and same material is used as spacer, so the number of process steps can be reduced. The work function of gate electrode is assumed to be 4.5 eV. The detailed process parameters considered for this study is listed in Table 1.

For numerical simulation of SOI JLFinFET shown in Fig. 3, 3D quantum transport equations are incorporated for accurate results using Synopsys Sentaurus device [22]. Drift diffusion approach is used for numerical simulation. As the higher doping concentration is used in

Table 1
SOI JLFinFET device Parameter considered for Process Flow.

Process parameters	**Values**
Gate Length (L_g)	20 nm
Fin Width (W_{fin})	10–24 nm
Fin Height (H_{fin})	10–24 nm
Gate Oxide Thickness (t_{ox})	0.9 nm
Channel Doping Concentration (N_D)	1×10^{18} cm^{-3}- 3×10^{19} cm^{-3}
Device operating temperature (T)	27–200 °C