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A 0.5-V 9.3-ENOB 68-nW 10-kS/s SAR ADC in 0.18-μm CMOS for biomedical applications

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ABSTRACT

This paper presents a 10-bit ultra-low power successive approximation register (SAR) analog-to-digital converter (ADC) intended for use in wearable biomedical circuits. In order to achieve the nanowatt range power consumption, an energy-efficiency modified V_{CM}-based switching scheme is proposed. In addition, a fully dynamic comparator and a dynamic register are used to eliminate the static power consumption. To improve the signal linearity in such a low supply voltage, a double-boost bootstrapped switch is proposed. A prototype of the proposed SAR ADC was fabricated in 0.18 μm 1P6M CMOS technology within a bio-sensor front-end circuit, which occupies an active area of 370×390 μm^2. The SAR ADC achieves 57.8 dB SNDR and consumes 68nW at 0.5 V supply voltage and 10 kHz sampling rate, resulting in a figure-of-merits (FOM) of 10.8fJ/conversion-step.

1. Introduction

In recently years, there is a growing interest in the development of integrated circuits for wearable and implantable biosensors, which provides remote health monitoring of a patient's state for a long period without any restriction on one's normal activities. Moreover, the wearable or implantable devices allow bio-signal monitoring to be done daily than limiting it within the clinical environment, which opens up the market for portable medical electronics to the ordinary people. Since these circuits are likely to be powered by portable batteries or energy harvest circuits, ultra-low power consumption is required to make it work normally for several years [1]. In a biosensor system, analog-to-digital converter (ADC) is the key building block which acts as a bridge between analog front-end and digital back-end [2]. Fig. 1 shows the block diagram of the biosensor system with a SAR ADC.

Conversion of the low-frequency bio-potential signals does not need high speed, but requires ultra-low-power operation for biomedical applications. Compared to other ADC architectures [2], successive approximation register (SAR) analog-to-digital converter (ADC) is an outstanding candidate for wearable or implantable biosensor due to its simple structure, energy efficiency and compatibility with technology scaling [3,4]. Work [3] proposed an ultra-low-power SAR-ADC with sampling rate of 40kS/s for wireless bio-potential network, which is based on a fully dynamic logic and consumes merely 97nW in 12-bit resolution. In addition, various schemes have been proposed to improve the SAR ADC power efficiency [5–8]. However, there are still several challenges to efficiently reduce the speed and bandwidth for ultra-low-power operation using inherently fast devices in advanced CMOS technologies.

Subthreshold operation has recently become an acknowledged solution for low-power applications because it significantly reduces the current consumption of the transistor [9]. In addition, the front-end system, with its scaled supply voltage, will be suitable for use in a wireless bio-potential SoC [1]. In order to achieve nanowatt range power consumption, the supply voltage is scaled to 0.5 V. Operating in the subthreshold region limits the circuit bandwidth. Fortunately, since the informal frequency spectrum of bio-signals lie at very-low frequency range, subthreshold operation does not affect the performance of the SAR ADC.

Since the frequency spectrum of bio-signals lie at low levels from sub Hertz to couple of hundred Hrtz, the sampling rate should be set to a higher value to achieve a better performance. However, large sampling rate results in large power consumption, thus the sampling rate should be set to a relatively small value to reduce the power consumption. Therefore, the sampling rate of this SAR ADC is set to 10k Hz based on the trade-off between SAR ADC performance and power consumption.

A dynamic comparator and a fully dynamic SAR logic are used to prevent the static power consumption. Moreover, a high power-efficiency modified V_{CM}-based switching scheme is proposed. Since the supply voltage is close to the MOSFET subthreshold voltage, a double-boost bootstrapped sampling switch is proposed to improve the ADC performance. The paper is organized as follows: Section 2 shows the overall SAR ADC architecture. Section 3 describes the capacitor switching procedure and analyzes its power and linearity. The key building blocks are discussed in Section 4. The measurement results

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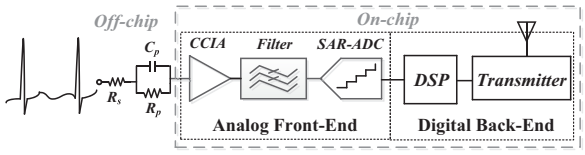

Fig. 1. Block diagram of the biosensor system.

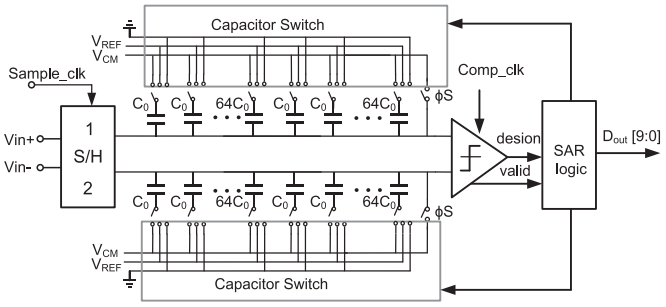

Fig. 2. Block diagram of the SAR ADC.

are given in Section 5. Finally, a conclusion is made in Section 6.

2. Overall SAR ADC architecture

Fig. 2 shows the block diagram of the proposed SAR ADC. It is implemented in a fully differential architecture to enhance the common-mode noise immunity and improve the linearity. The SAR ADC comprises a bootstrapped sampling switch, a binary weighted capacitive DAC, a dynamic latch comparator and a low-leakage synchronous SAR logic. The input signal is sampled on the top-plate nodes of the capacitor array by bootstrapped switches, and the comparator compares the voltage on the differential capacitor arrays and generates the corresponding digital code. The output digital codes of comparator are stored in the SAR logic, which in turn feedbacks control signals to the DAC switching array. The ADC repeats this procedure until all 10 bits are decided. Fig. 3 shows the input clocks and the waveforms of the capacitor array top-plate notes during the switching procedure. The common-mode voltage is equal to V_{CM}, and thus reduces the signal dependent dynamic offset of the comparator [8], which makes the design of the latch comparator easier.

Since all the building blocks are dynamic, there is no static power consumption, and thus the energy is greatly reduced in such a low sampling rate. Moreover, the absence of any residue generation and transfer enables a SAR ADC to employ rail-to-rail signal swing [10], thus a higher SNR is achieved. Supply voltage scaling is an efficient technique to reduce both the switching and leakage power consumption, especially at low speed operation [11]. In addition, since the DAC capacitor array voltage swing decreases with the power supply voltage, the energy consumed by DAC is reduced. However, ultra-low supply voltage brings several challenges when designing a high-performance ADC, such as the linearity, dynamic range and noise immunity [8].

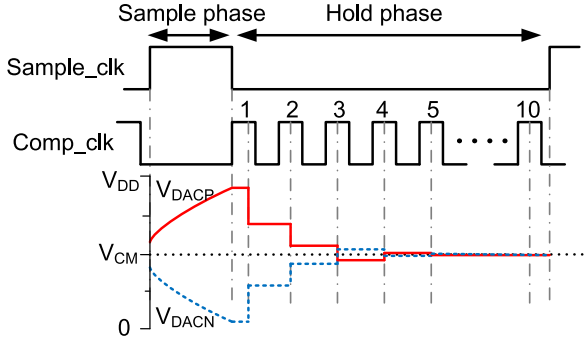

Fig. 3. Clocks and DAC top-plate waveform during the switching procedure.

3. Capacitor switching procedures

3.1. Modified V_{CM}-based switching scheme

In recent years, biomedical applications are drawing the research attention, and many outstanding switching schemes are proposed to improve the power efficiency of SAR ADC. However, most of these works consider only the current switching energy while ignoring the reset energy for next conversion step, which are not practical in reality. Several excellent works take both of switching energy and reset energy into consideration and still achieve a good reduction of the energy [5,6]. Work [12] proposed a split capacitor array to improve the speed and power efficiency. Work [13] proposed a common-mode based charge recovery switching method to reduce the switching energy and improve the conversion linearity. Work [14] combined these two techniques and proposed an energy-efficient and highly-linear capacitance-split V_{CM}-based switching capacitor scheme for SAR ADC, in which the MSB capacitor is split into an identical copy of the rest of the capacitor array. The schematic of the capacitance-split V_{CM}-based switching capacitor scheme is shown in Fig. 4. The switching algorithm reduces the number of capacitors by half compared with the conventional scheme. In addition, it achieves 37% less switching energy and 2 times better INL than that of the V_{CM}-based one [14].

The capacitance-split V_{CM}-based scheme reduces the total capacitor by half when compared with the conventional switching scheme. However, the total single-end capacitance is $512C_0$ for a 10-bit ADC, which is still too large and takes large area and consume high power. In order to further reduce the area and power consumption, a modified V_{CM}-based scheme is proposed. Fig. 5 shows the last 4 bits switching procedures of the modified V_{CM}-based switching algorithm.

The proposed switching algorithm is the same as the capacitance-split V_{CM}-based scheme except the last bit. In the sampling phase, the bottom-plates of capacitors are initially loaded with the sequence of [V_{CM}, V_{CM} ..., V_{CM}]. In the meantime, the top-plates sample the differential inputs V_{ip} and V_{in}. During the conversion phase, the input values are sampled on the top-plates of the capacitors, and the comparator compares the voltages on two capacitor arrays when the "Comp_clk" is set to "1". The switching procedure follows the capacitance-split V_{CM}-based switching algorithm before the last bit decision. In order to achieve the last bit, the LSB capacitor of the Main-subarray is used. We just change the LSB capacitor of the V_{ip} capacitor array using V_{CM}-based switching algorithm, shown in Fig. 5. Through this way, the total capacitance of a single-end is reduced to $256C_0$, which saves 75% total capacitor compared with the conventional switching scheme, and thus energy and area are greatly reduced.

3.2. Switching energy analysis

It is instructive to calculate the switching energy of the proposed switching scheme. For alleviating the computation, 4-bit switching procedures are taken as an example, shown in Fig. 5. All possible

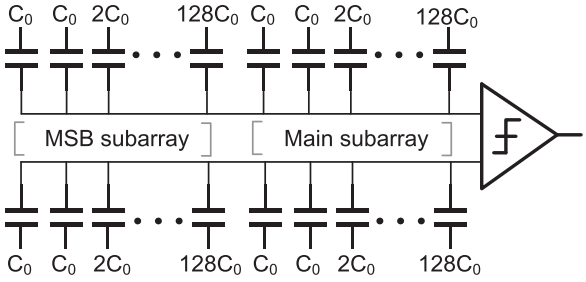

Fig. 4. Schematic of the capacitance-split V_{CM}-based switching capacitor scheme.