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An implementation of an electronic tongue system based on a multi-sensor potentiometric readout circuit with embedded calibration and temperature compensation

Wen-Yaw Chung [a,*], Angelito A. Silverio [a], Vincent F.S. Tsai [b,c], Cheanyeh Cheng [d], Shu-Yu Chang [a], Zhou Ming-Ying [a], Chi-Ying Kao [d], Si-Yuan Chen [e], Dorota G. Pijanowska [f], Dan Rustia [a], Yi-Wen Lo [a]

[a] *Department of Electronic Engineering, Chung Yuan Christian University, Chung-Li District, Taoyuan County 32023, Taiwan, ROC*
[b] *Ten-Chen Medical Group, Chung-Li District, Taoyuan City 32023, Taiwan, ROC*
[c] *Department of Biomedical Engineering, Chung Yuan Christian University, Chung-Li District, Taoyuan City 32023, Taiwan, ROC*
[d] *Department of Chemistry, Chung Yuan Christian University, Chung-Li District, Taoyuan City 32023 Taiwan, ROC*
[e] *Jimei University, Xiamen City, China*
[f] *Institute of Biocybernetics and Biomedical Engineering, Polish Academy of Sciences, Warsaw, Poland*

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ABSTRACT

We present an electronic tongue system composed of an analog front-end (AFE) with embedded calibration and temperature compensation for interfacing with an array of Ion-Sensitive FETs (ISFETs) or Enzyme – Extended Gate FETs (EEGFET). The AFE consists of a floating bridge type constant voltage constant current (CVCC) structure, and transmission gates as sensor enable. It also includes a temperature readout circuit and an instrumentation amplifier for temperature compensation. The calibration algorithm is synthesized into a Field Programmable Gate Array (FPGA) and implemented onto an Application Specific Integrated Circuit (ASIC). The system shall be used to measure the pH and the concentration of calcium ions in a solution alongside a conductometric sensor system. The ISFETs used are from ITE-Poland and shall be utilized to measure pH; meanwhile, to measure the Ca^{2+} concentration, EEGFETs with calcium ionophore on polyvinyl chloride (PVC) on SnO_2/ITO/Glass thin film have been fabricated. The performance of the system using pH buffer solutions of pH 4–10, and $CaCl_2$ buffer concentrations of 0.001–1 M has been verified. The sensors and the AFE readout exhibited a Nernstian response (~50 mV/pH) with a very stable output having a relative standard deviation of just ~ −0.4%, and a Ca^{2+} sensitivity of 25.02 mV/pCa, with a drift of −6.82 mV/M-s. An on-chip version of the AFE using TSMC 0.35 μm CMOS 2P4M Technology is also presented as well as the ASIC implemented on TSMC 0.18 μm CMOS 1P6M technology.

1. Introduction

Urolithiasis or urinary stone formation is one of the highly impacting factors in our society and has evolved to a widespread disease for the past 3 decades. It is said that about 10% of people will experience kidney stones in their lifetime and about 50 – 70% of those will have recurrences [1]. Furthermore, for those who have this history, there is a 10% cumulative chance of recurrence for each year after the first stone formation [2]. The economic loss of the society attributed to *urolithiasis* is estimated to be up to billions of US dollars [3]. Urolithiasis prevention not only mitigates the patients' condition but also reduces health expenses [4].

The latest and well accepted factors causing urolithiasis are: 1. Primary precipitation of calcium phosphate (CaP) at high nephron levels; 2. CaP dissolved in low urine pH; 3. High ion-activity products of CaOx (supersaturation); 4. Low pH, low citrate and high ion-strength of urine causing large CaOx crystals; and 5. anatomical, as well as hydrodynamic factors pertaining to stone retention [5]. Several methods of assessing the risk of crystallization and recurrent stone formation has been detailed in [6]. One such method is the bonn-risk index which is based on the potentiometric detection of the ionized calcium (Ca^{2+}) together with an optical determination of the triggered crystallization of CaO in unprocessed urine [6]. By combining measurements of pH and Ca^{2+}, a platform can be built to aid in urinary stone prediction. To implement this, the proponents propose an electronic tongue system which utilizes a sensor array consisting of ion sensitive

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[*] Corresponding author. Tel.: +886 2654615.
E-mail address: eldanny@cycu.edu.tw (W.-Y. Chung).

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field effect transistors (ISFETS), and enzyme extended gate FETs (EEGFETs) for the detection of pH and Ca^{2+}. The system has been implemented on-board with a digital back-end that controls the analog front-end (AFE) sensor interface and performs calibration. The AFE and the Application Specific IC (ASIC) has been implemented on-chip using TSMC 0.35 μm CMOS 2P4M, and TSMC 0.18 μm CMOS 1P6M technology, respectively.

This paper is organized as follows: Section 1 presents the background information about *urolithiasis* to which this system shall be utilized; Section 2 discusses the operating principles of the two FET sensors, the AFE interface circuits for potentiometric biosensing as presented in literature and the proposed AFE readout circuit design offering interface to multi-sensor arrays; this section will also present the synthesized ASIC on FPGA; Section 3 presents the experimental results of the on-board module with the ASIC, as well as the HSPICE simulation results of the on-chip version along with its compensation sub-circuits. An ISFET behavioral macro-model has been used to verify the AFE on-chip's performance. Section IV presents the conclusion and future works.

2. FET sensors and potentiometric readout circuit

2.1. Ion sensitive semiconductor sensors

The Ion-Sensitive and Enzyme Extended Gate FETs are similar to the MOSFET except that the effective gate material has been modified from polysilicon into an ion sensitive membrane layer. The materials for this layer are summarized in Table 1. Both FETs utilize a reference electrode (Ag/AgCl) that effectively forms the gate immersed in the solution under test (SUT) alongside the ion sensitive membrane of the FET. A potential difference is created between the reference electrode (RE) and the membrane as described by the Nernst equation:

$$E=E_0+\left(\frac{2.303RT}{nF}\right)\log(a_i) \tag{1}$$

where: E is the total potential between RE and the sensing membrane, E_0 is the potential of the RE, $(2.303RT/nF)$ is the Nernst factor, and a_i is the ionic activity of ion i. The Nernst factor consists of the gas constant (R), the temperature in Kelvin (T), Faraday's constant (F) and the charge of the ion (n).

The governing equations for these FET-based ion sensors follow the drain current equation of a MOSFET except that the threshold voltage (V_{TH}) is a function of the ion concentration. These FETs are normally operated in the linear region and is thus described in [8] by the following equations:

$$I_{DS}=\mu_n C_{ox}\frac{W_{eff}}{L_{eff}}\left[\left(V_{GS}-V_{TH}^{*}\right)V_{DS}-\frac{1}{2}V_{DS}^{2}\right] \tag{2}$$

$$V_{TH}^{*}=V_{TH}-E_{ref}-\frac{RT}{n_iF}\ln(a_i) \tag{3}$$

Table 1
H^+ ion Sensing Materials [7].

Material	***Sensitivity*** (mV/pH)	***Range*** (pH)	***Hysteresis*** (mV)	***Drift*** (mV/h)
SiO_2	37–48	4–7	Unstable	Unstable
Si_3N_4	46–56	1–13	3	1
Al_2O_3	53–59	1–13	0.8	0.1–0.2
Ta_2O_5	56–59	1–13	0.2	0.1–0.2
$PbTiO_3$	53–58	2–12	3 – 5	0.5–1
SnO_2	56–58	1–12	1.91	–

where: C_{OX} is the oxide capacitance; $\mu_n$is the carrier mobility, W_{eff}/L_{eff} is the MOS' aspect ratio (W_{eff} - effective width, L_{eff} - effective length), E_{ref} is the reference electrode potential relative to vacuum, and a_i is the ionic activity. Note that the factor $\mu_n C_{ox}$ is usually denoted as K_p which is the transconductance parameter. The cross-sections of the ISFET and EEGFET used are shown in Fig. 1. The ISFETs are obtained from Instytut Technologii Elektronowej (ITE) Poland and has the following specifications: $W=600$ μm, $L=16$ μm, both SiO_2 and Si_3N_4 gate layers are 65 nm thick [9]. An exemplary I_D-V_{GS} ISFET characteristic for different pH buffer solutions with $V_{DS}=0.5$ V is shown in Fig. 2. To obtain the threshold voltage, a line tangent to the I_{DS} curve (blue trace) is obtained at the maximum transconductance (G_M). The x-intercept of this line gives the V_{TH} value. G_M is defined as in Eq. (4) for a typical NMOS:

$$G_M=\frac{\partial I_{DS}}{\partial V_{GS}}=\mu_n C_{ox}\frac{W_{eff}}{L_{eff}}(V_{GS}-V_{TH})=\frac{2I_{DS}}{V_{GS}-V_{TH}} \tag{4}$$

The ISFET has achieved an average sensitivity of 45.6 mV/pH using 12 ISFETs from ITE Poland. Meanwhile, prior to depositing the membrane containing Ca^{2+} ionophore onto the thin film, the response of the EGFET to pH has also been verified. The EGFET has achieved an average sensitivity of 53.2 mV/pH for five sensing membranes consisting of SnO_2/ITO thin films of similar areas.

The Ca^{2+} sensing membrane of the EEGFET consists of the thin film of SnO_2/ITO/Glass with an immobilized Ca^{2+} ionophore on Polyvinyl Chloride (PVC) atop it. The ionophore (A23187) and PVC are obtained from Sigma Aldrich. The CD4007UBE MOSFET was used to form the EGFET. This chip consists of 6 MOS elements (3 NMOS and 3 PMOS) which have a $|V_{TH}|$ of 1.0–1.2 V.

2.2. Potentiometric readout circuit for FET array interface

Several potentiometric sensor readout circuits have been suggested in literature [8,10–18]. Two approaches reported in literature involve either the floating source [10–12] or the floating gate [8,13,14]. These structures are shown in Fig. 3. In publications [10,12] a floating source and bridge – type constant voltage and constant current potentiometric AFE core with V_{TH} extractor sensor and difference amplifier for temperature compensation were reported. Another implementation utilized a source-drain follower where the output voltage is equivalent to the input potential at the extended gate; this topology resulted in an output that is independent of device parameters such as threshold voltage and operating temperature. Furthermore, this approach has been implemented to create an integrated sensor array that consumes small area and low power [15]. In work [16] demonstrated solution based on integration of an ISFET sensor with a contact imaging sensor into an array for removing cross-talk between sensor cells resulting in higher pH reading accuracy. The circuit consisted of dual mode sensor arrays with the corresponding switching circuitry and a global switched capacitor operational amplifier. The implementation utilized a differential difference amplifier-based second generation current conveyor (DD-CCII) as a readout circuit to the potentiometric sensors, and has been implemented in a self-powered wireless sensor network for monitoring contaminants and hydric systems [17]. In this approach the floating source bridge circuit with array interfacing feature, on-chip temperature sensor and a current-mode instrumentation amplifier (IA) was utilized. This readout can interface an array of FET sensors via the transmission gate. For effective temperature compensation, the IA has been used due to differential high input impedance and high common-mode rejection ratio (CMRR), necessary.

The potentiometric readout circuits usually applies a constant voltage and constant current (CVCC) to the FET-based sensor. For the floating source (see Fig. 3a), the constant voltage is set up by the V_{REF} and the voltage divider network of R_1 and R_2; the constant