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Pin-pin ESD protection for electro-explosive device under severe human body ESD

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ABSTRACT

Electrostatic discharge (ESD) may introduce huge damages to electro-explosive devices (EEDs). This paper studies the pin-pin ESD protection for EED under server human body ESD. We use the PSpice and MATLAB to simulate the ESD of EED protected with transient voltage suppressor (TVS), varistor, semiconductor arrester and capacitance. Moreover, we achieve the decay time, current waveforms, voltage waveforms and energy integration waveforms of the EED during the ESD, with different protections. Simulation results reveal that TVS succeeded in protecting bridgewire EED against the pin-pin ESD, while other three did not provide adequate protection. The pin-pin ESD experiments have been performed using the TVS and varistor. Experimental results show that, using the TVS protection, the EED is not firing under the severe 50 kV ESD voltage. However, by using varistor protection, the ESD protection capability increases by more than 90%, while the protection capability only enhances by 3.1%. The response time of the TVS, i.e. 10^{-12} s, is much faster than that of the varistor, i.e. 10^{-8} s.
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1. Introduction

It is reported that there are unexpected accidents in the electro-explosive device (EED) or weapons systems due to the electrostatic discharge (ESD) every year. ESD may be introduced during the production, assembly, transport, testing, and operation of the EEDs and weapon systems. The harms of ESD is very universal which mainly occurs to the human body and equipment [1–3]. The EED which meets the military standard requirements also presents unexpected fire accident. The reason is that the severe human body ESD is beyond that of the military standard. This shows the significance of the study on the protecting EED from severe human body ESD through pin-pin.

The most severe human body ESD voltage value is 25 kV, in the industry and military standards [4–6]. Other relevant methods of EED's ESD experiments for evaluating the safety and standards are conducted in accordance with the above criteria. Many works related to ESD protection have been performed based on the above criteria. Many countries reported the highest body ESD voltage of 40–50 kV, and Professor Shanghe Liu suggested that human body ESD voltage could reach up to 50 kV [7–9]. Up to now, almost all experiments for ESD hazards and protective measures are carried out on 25 kV [10–13], where most ESD protection researches have focused on the pin-case. In contrast, a few research on the ESD protection using the pin-pin have been reported [14,15]. Chen Fei, used the varistor for protecting the semiconductor bridge initiators against the ESD, while the semiconductor bridges are insensitive pyrotechnics [16–19]. However, the protection for sensitive EED against the severe human body ESD has not yet been reported. In the other side, it has not yet been analyzed whether the protection can meet the requirements for the voltage of human body ESD model is up to 50 kV or not.

Several research works on the ESD protection have been accomplished in the Sandia Laboratories [20,21]. For instance, a parallel capacitor and zener diode were used to protect semiconductor bridge initiators against the pin-to-pin ESD by King et al. [20]. The experiments showed that use of a 1 μF capacitor and 14 V Zener diode may protect the semiconductor bridge from the pin-pin ESD, while the protection circuits had no effect on the semiconductor bridge's threshold voltage. Afterwards, Weinlein et al. used a TVS as a protective device in the ESD protection for a laser diode ignited actuator [21]. Sandia's human model and the PSpice software were used as the circuit simulation software in the above two studies. The ESD network and the load circuit are combined to establish a circuit model to simulate different effects with different ESD protection components. However, there is little study on the pin-pin ESD protection with TVS for EED under server human body ESD.

The pin-pin ESD firing is an electric heating process. The methods for making the EED insensitive may raise the firing threshold voltage of the EED, leading to a decline in firing sensitivity of the EED and raise normal firing threshold voltage of the EED. Therefore, to meet the low firing threshold voltage, the shunting EED energy method is used to prevent pin-pin ESD events. The devices shunting the pin-pin ESD energy require to quickly absorb most of the ESD energy in the high-pressure ESD. In the normal role of the EED, the device is similar to the "disconnect" state which does not affect the normal combustion performance of the EED. Besides, the ESD shunt devices have TVS and varistor [22].

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In this paper, we use the DR-2 electric detonator as a sample which is a sensitive electric product, with the product size of Φ5.1 × 8 mm. Moreover, the electrode plug size is Φ4.22 × 4 mm and the bridgewire diameter is 10 μm Pt&W alloy. We use the bridgewire resistance of 3–9 Ω, the firing voltage of 12 V, with a 6.8 μF capacitor. The excitation energy of the EED is 4.9×10^{-4} J in normal condition. The experimental results show that the pin-pin ESD voltage is 18.45 kV, where the voltage of the EED is 22.14 V and the peak power is 88.6 W.

2. Simulation

2.1. Modeling and verification of the PSpice simulation

In this paper, we analyze the current waveform of the simulation and standards. The ESD circuit model is validated using both simulation and experiment. The human body ESD model instrument is designed as the experimental test equipment. The maximum human body ESD voltage can reach up to 50 kV. Fig. 1 shows the ESD instrument.

(A). Verification of the standard current waveform

The human body ESD model may be represented by a single RC model with resistance R ($R = 5$ kΩ) connected in series. Sandia single RC ESD model is established by PSpice. Fig. 2 shows the current-time waveforms of the simulation, with charging voltage of 25 kV, and the standard GJB5309.14-2004.

Fig. 2 compares the current-time curve, achieved from the ESD instrument, with the standard current-time curve. We see that the shape and trend of the waveform are in agreement, where the rise and decay times are the same. The peak current error of the single RC series 5000 Ω model is 1%, and the maximum current error is 2.7% in the decay time. The ESD model by PSpice is credible by the parameters such as waveform shapes, rise time, decay time, relative error of the peak current and maximum relative error of the current in decay time.

(B). Experimental demonstration

In this section, we accomplish the ESD experiments using the ESD instrument according to standard [4]. Fig. 1 shows the ESD instrument. To follow standard [4], we consider the ESD analog circuit requirements, i.e. a 500 pF capacitor charge with a 5kΩ series resistance of the ESD products discharge. First, we charge the capacitor to 20 kV, and then, perform the ESD experiment. The same ESD conditions are considered for the simulation with PSpice software.

Fig. 3 compares the simulation and experimental results for the current in a single series RC of 5000 Ω–20 kV. It may be seen that the EED current achieved using the PSpice is close to the experimental one. The current declines, exponentially, after reaching to its peak, which is consistent with the theoretical results. The error of the peak current is only 3.85%. The relative error of the circuit is 6.8% at the decay time. The error between the simulation and experimental results is reasonable which shows the validity and accuracy of the simulation.

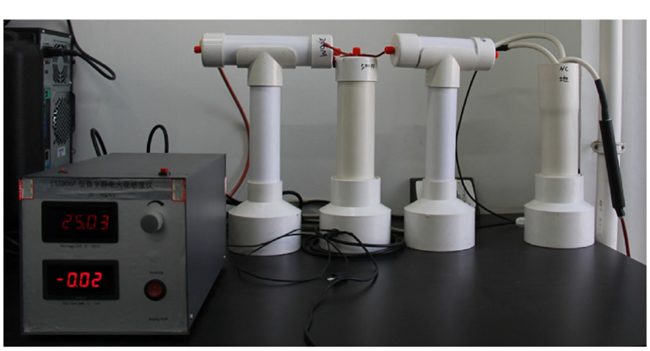

Fig. 1. Single RC ESD instrument.

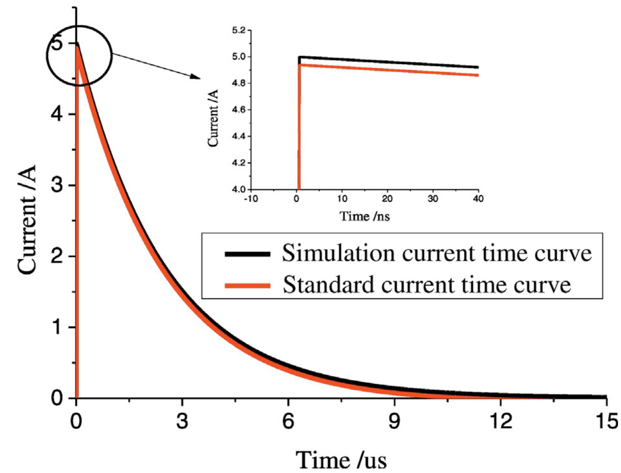

Fig. 2. Single RC, series 5000 Ω–25 kV, simulation with standard current-time curve.

2.2. TVS selection method

The TVS selection should consider the following aspects for the pin-pin ESD protection of the EED.

(1). The actual ESD in pin-pin is possibly positive with negative current direction. Therefore, we choose the bidirectional TVS.
(2). To protect the normal work of EED from the TVS diversion, the maximum reverse voltage, V_{RWM}, of the TVS should be greater than the normal working voltage of the protected device.
(3). The clamping voltage, Vc, of the TVS represents the maximum limit voltage. To effectively protect the device, the clamping voltage should be less than the ESD damage voltage of the protected device.
(4). The peak power should comply with the TVS and the ESD power diagram, as it is shown in Fig. 4, otherwise it may damage the TVS.
(5). The response time is the time when the TVS voltage reaches the working voltage, beginning to play a protective role. It must be less than the ESD time.

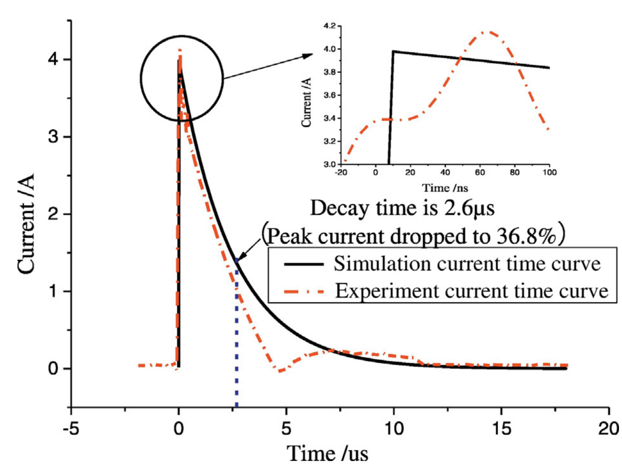

Fig. 3. Simulation and experimental results for the current of a single series RC circuit of 5000 Ω–20 kV simulation.

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