Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Effect of interface traps for ultra-thin *high-k* gate dielectric based MIS devices on the capacitance-voltage characteristics

Slah Hlali [a,*], Neila Hizem [a], Liviu Militaru [b], Adel Kalboussi [a], Abdelkader Souifi [b]

[a] Laboratoire de Microélectronique et Instrumentation (LR13ES12), Faculté des Sciences de Monastir, Université de Monastir, Avenue de l'environnement, 5019 Monastir, Tunisia
[b] Institut des Nanotechnologies de Lyon — site INSA de Lyon, UMR CNRS 5270, Bât. Blaise Pascal, 7 avenue Jean Capelle, 69621 Villeurbanne Cedex, France

ARTICLE INFO

Article history:
Received 25 February 2017
Received in revised form 24 June 2017
Accepted 24 June 2017
Available online xxxx

Keywords:
Al_2O_3/Si interface
High-k
Metal/insulator/semiconductor (MIS)
Numerical simulation
Interface state density
C-V characteristics

ABSTRACT

The impact of states at the Al_2O_3/Si interface on the capacitance-voltage C-V characteristics of a metal/insulator/semiconductor heterostructure (MIS) capacitor was studied by a numerical simulation, by solving Schrodinger-Poisson equations and taking the electron emission rate from the interface state into account. Efficient computation and accurate physics based capacitance model of MOS devices with advanced ultra-thin equivalent oxide thickness (*EOT*) (down to 2.5 nm clearly considered here) were introduced for the near future integrated circuit IC technology nodes. Due to the importance of the interface state density for a low dimension and very low oxide thickness, a high frequency C-V model has been developed to interpret the effect of interface state density traps which communicate with the Al_2O_3/Si and their influence on the C-V characteristics. We found that these states are manifested by jumping capacity in the inversion zone, for a density of interface, higher than 1×10^{11} cm^{-2} eV^{-1} during a p-doping of 1×10^{18} cm^{-3}. This behavior has been investigated with various doping, temperature, frequency and energy levels on the C-V curves, and compared with the MIS structure that contains a standard SiO_2 insulator.

1. Introduction

Metal-oxide-semiconductor (MOS) structures play a crucial role in many devices, especially in microelectronics and optoelectronics. The performance and reliability of MOS devices are strongly dependent on the formation of insulator layer (native or deposited), interface states (N_{ss}) localized at the semiconductor-insulator interface and the series resistance (R_s). The electrical and dielectric properties of these devices strongly depend on the applied voltage, frequency and temperature.

The continued reduction of device size has now necessitated the diminution of the thickness of the gate oxide layer to a few nanometers in order to maintain the same degree of gate control over the channel from a high leakage current [1]. In order to surmount this limitation, high-k (high dielectric constant) materials are being introduced to achieve a greater physical thickness and thus reduce the direct tunneling current while retaining a low oxide thickness [2,3]. Thus, replacing SiO_2 with high-k materials is the prime technological challenge. In recent years there has been a growing interest in metal oxides as dielectric materials for gate oxides of MOSFETs and stable capacitors in ultra large scale integrated electronic circuits (ULSI). Extensive research is now in progress to find another insulator with a higher dielectric constant, large band gap, significant conduction band offset and high breakdown strength for use in sub-100 nm silicon technology [4,5]. New dielectric conductor combinations should be tuned for the right metal work function as well as the optimum thermo-chemical stability of the layer stack. Hence, much effort has been made to explore new combinations of dielectric and conductive layers so that miniaturization of MOS-based devices can be continued following Moore's law. The combination TiN/Al_2O_3 has been identified as a promising and especially reliable candidate thanks to its chemical compatibility and thermal stability, good adhesion properties on various substrates, and low interface trap densities in TiN/Al_2O_3/p-Si devices [6]. Furthermore, both materials can relatively be easily synthesized by atomic layer deposition (ALD) under compatible processing conditions. Al_2O_3 is known for its modest dielectric permittivity of ~9 and the high breakdown of electric field due to its large band gap (9 eV) [7,8]. Moreover, it has a large band offset with Si, which is crucial in maintaining low leakage currents through devices [9]. The metal TiN is a well-established midgap, with a low electrical resistance. Therefore, it is commonly used as an electrode material that blocks the out diffusion of Si more efficiently than Al.

Previously, the introduction of nanoelectronics puts a barrier in determining the nature of the MOSFETs with ultra-thin oxides as a result; nowadays it is a matter of significance to consider the interface states during MOS operation. Traps at the silicon-oxide interface play a significant role in determining the threshold voltage and inversion layer

* Corresponding author.
E-mail address: hlalislah@yahoo.fr (S. Hlali).

http://dx.doi.org/10.1016/j.microrel.2017.06.056
0026-2714/

mobility. Proper MOS device modeling requires the knowledge of the density of interface states throughout the band gap.

It is true that studies of interface states for MOS structure has required a great attraction for several years. However, scientific research in this branch of electronics continues to be attractive and fascinating among researchers today [11–14].

For example, Pengkun et al. [13] has studed the impact and origin of interface states at the monolayer MoS_2 and HfO_2 high-k gate dielectric interface. They found that the presence of sulfur vacancies is responsible for the generation of interface states that causes the frequency dispersion in the accumulation regime of the MoS_2 MOSCAP, which exhibits a dependence on the applied gate voltage.

However, carrier transport study with an integrated high-k gate dielectric (Al_2O_3) have not been reported so far. In particular, the electrical characteristics such as capacitance-voltage (C-V) temperature dispersion and its dependence on interface states density (D_{it}) which influence the carrier transport properties deserve a further investigation.

In this paper, the interface charge densities have been measured for MIS devices using high-k material. We have worked and analyzed on selected high-k material: Al_2O_3 the values of D_{it} for this material and compared with the standard SiO_2 based MOS devices for constant insulator thickness.

We present a theoretical study through a bi-dimensional simulator ATLAS [15], to investigate capacitance-voltage characteristics with and without the interface state density of metal insulator (high-k: Al_2O_3) semiconductor (p-Si) devices.

We report on the effect of bias voltage, silicon substrate doping concentration and that of frequency and temperature on the electrical and dielectric properties of TiN/Al_2O_3/p-Si structure in which the Al_2O_3 dielectric layer is deposited by ALD. Our approach is based on the numerical simulation self-consistly solving the Schrodinger-Poisson equations using a finite-difference method with non-uniform mesh sizes.

2. Device characteristics

The MIS capacitor used during the simulations performed for this study is composed of a Titanium nitride gate, an Al_2O_3 insulator layer with $T_{OX} = 5$ nm and a P-type silicon substrate with a doping concentration $N_A = 1 \times 10^{18}\ cm^{-3}$. The surface of our MIS structure is assumed to be $100 * 100\ \mu m^2$ during all bi-dimensional simulations, as presented in Fig. 2.

A DC voltage (V_G) was applied to the capacitor gate, varying from −3 V to 2 V and the AC study of high frequency C-V curve was performed, maintaining frequency at 1 kHz for all simulations.

3. Theoretical analysis

The gradual evolution of microelectronics in recent years was accompanied by a reduction in the thickness of the oxide (gate oxide in the case of the transistors), which resulted in physical or technological problems. Other oxides have been proposed and more particularly oxides with a high dielectric constant, the “high-k”. Indeed, thanks to these larger dielectric constants, one can keep a fixed oxide thickness while increasing the gate-channel coupling capacitance of the transistor [16]. To replace SiO_2, the high-k oxides must meet certain criteria in terms of the value of permittivity, band structure, discontinuity bands for the transport of loads, thermodynamic stability, quality of the interface with the Si, morphology, compatibility with the gate electrode and with the technological process, reliability, etc.

The following table (see Table 1) provides a comparison with different characteristics as dielectric constant k, band gap, conduction band (CB) offset to Si, and tunneling effective mass (m^*) for the oxide materials between the SiO_2 and a high-k oxide:

The interface states can be estimated by measuring their densities noted D_{it} or N_{ss}. This density describes the number of defects at the electrically active interface per unit area and energy ($cm^{-2}\ eV^{-1}$). The density of interface states often indicates the quality of the used technology.

Based on a self-consistent solution of Schrödinger and Poisson equations, we determined a theoretical C-V curve from a metal/Al_2O_3/Si structure. The quantized energy levels E and their corresponding electronic wave functions ψ satisfy Schrödinger's equation. The one dimensional Schrödinger equation is given by

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left[\frac{1}{m^*(x)}\frac{d}{dx}\right]\psi(x) + V(x)\psi(x) = E\psi(x) \tag{1}$$

In Eq. (1), $\hbar$ is the reduced Planck constant, m^* represents the electron effective mass, ψ is the carrier wave function, E is the electron (or hole) potential energy and $V(x)$ is the potential energy profile of the barrier conduction band (or valence band).

The potential energy profile of the barrier conduction band or valence band $V(x)$ in the Schrödinger Eq. (1) is linked to the electrostatic potential $\varphi(x)$ via the relation:

$$V(x) = \pm\left(-q\varphi(x) + \Delta E_{C,V}\right) \tag{2}$$

where $\Delta E_{C,V}$ is the band offset between the conduction or valence band of the semiconductor and conduction or valence band of the oxide. $\varphi(x)$ is then calculated with the one-dimensional Poisson equation.

$$\frac{d}{dx}\left(\varepsilon(x)\frac{d}{dx}\right)\varphi(x) = -\frac{q}{\varepsilon_0}(p(x) - n(x) - N_A + N_D) \tag{3}$$

where q is the electronic charge, $\varepsilon(x)$ is the relative dielectric constant, ε_0 is the permittivity of a vacuum, N_D and N_A are ionized donor and acceptor concentrations, respectively. $\varphi(x)$ is the electrostatic potential and $n(x)$ and $p(x)$ are the free electron and hole concentrations, respectively. These free-carrier concentrations are obtained from the following equations [5]:

$$n(x) = \frac{qKT}{\pi\hbar^2}\sum_{i,j}\sum_{K=1}^{nlevel} m_{2D}^{i,j} g_{i,j} \times \left|\psi_{i,j}^{K}(x)\right|^2 \times \ln\left\{1 + \exp\left[\left\{-\beta\left(E_{i,j}^{K}(x) + \varphi_F\right)\right\}\right]\right\}$$
$$p(x) = \frac{qKT}{\pi\hbar^2}\sum_{lh,hh}\sum_{p=1}^{plevel} m_{2D}^{lh,hh} g_{lh,hh} \times \left|\psi_{lh,hh}^{p}(x)\right|^2 \times \ln\left\{1 + \exp\left[\beta\left(E_{lh,hh}^{p}(x) + \varphi_F\right)\right]\right\} \tag{4}$$

where subscripts i and j refer to longitudinal and transverse electrons in the conduction band of the semiconductor, $m_{2D}^{i,j}$ is the two-dimensional density of states effective mass and $g_{i,j}$ is the number of equivalent valleys corresponding to the longitudinal and transverse electrons, respectively, subscript K refers to the different modes considered in the simulation, $E_{i,j}^{K}(x)$ is the Kth (i or j) carrier energy subband induced by the quantum confinement, $\psi_{i,j}^{K}(x)$ is the corresponding normalized wave function, φ_F is the difference between the middle of the

Table 1
Material properties of SiO_2 (standard) and Al_2O_3 (high-k).

Oxide	Constant dielectric K	Band gap [eV]	CB offset [eV]	Stability thermal compared to silicon	m^*/m_0
SiO_2 (standard)	3.9	9	3.15	>1050 °C [18]	0.5 [19]
Al_2O_3 (high-k)	9	8.8	2.8	~1000 °C [18]	0.35 [19]

Please cite this article as: S. Hlali, et al., Effect of interface traps for ultra-thin *high-k* gate dielectric based MIS devices on the capacitance-voltage characteristics, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.06.056