Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

A high fault coverage test approach for communication channels in network on chip

Babak Aghaei

Department of Computer Engineering, Malekan Branch, Islamic Azad University, Malekan, Iran

ARTICLE INFO

Article history:
Received 19 February 2017
Received in revised form 28 June 2017
Accepted 3 July 2017
Available online xxxx

Keywords:
Network on Chip
Communication test
Fault detection
Fault location
Test coverage
Fault coverage

ABSTRACT

This paper proposes a new high fault coverage test approach for short faults in Network on Chip communication channels. The proposed approach consists of a built in self-test as well as a Packet/flit Comparing Module (PCM) embedded in the network adapter and a router, respectively. The approach is mainly characterized by the fact that, the detection, location, and routing table updating processes are simultaneously carried out after which the test time is minimized. The approach with high scalability leads to 100% test coverage and 89.5% capability of diagnosing faulty channels in one round (two phases). The simulation results show that the approach hardware and time cost is optimized compared with the previous methodologies.

1. Introduction

Network on-Chip (NoC), being replaced with the outdated buses in NoC, has been supplied to the today's world demand for crowded computations [1,2]. NoC possesses a packet-switched structure and consists of numerous router and communication channels which are in charge of routing the packets and communicating routers, respectively. The Intellectual property (IP) cores are connected to the communication infrastructure through Network Adapter (NA) [3]. Having such exclusive characteristics as wiring resources, diverse traffic pattern, heterogeneous components integration, optimal power consumption, scalability, resources reusing, Fault tolerance and testability have made NoC a functional approach to oppose the bottlenecks in the communications Systems on Chip (SoCs) [4].

After its production process, NoC in its lifetime is exposed to a wide variety of faults which result in such malfunctions as data losing, efficiency degradation, and eventually, entire system breakdown. Fault Tolerance is the capability that enables NoC-based SoCs to pursue their functions despite the faults. The approaches proposed for NoC fault tolerance can be classified into two categories: 1) approaches adding hardware on NoC to tolerate potential faults such as fault detection and diagnosis codes, retransmission, alternative routes, Triple Module Redundancy (TMR), and spare routers [5], 2) approaches adding logic to the NoC to track the alternative route. This logic being proposed in a tolerable routing algorithm put a noticeable impact on tolerating permanent faults and improves NoC-based SoCs reliability [6]. The faults, however, must be detected and located using test mechanisms before performing anything for NoC Fault tolerance [7].

Generally, the test of an NoC-based SoC for detecting is usually divided into two parts: the test of the IP cores and the test of the communication infrastructure [8]. The test of the cores is typically based upon the reuse of the NoC as TAM to reduce the test overhead. There are hard works that are carried in this field [9–12]. The test of the communication infrastructure encompasses routers test and communication channels test. A bulk of investigations e.g. [13–19] has been conducted to test the routers. A substantial number of investigations have been conducted in the field of communication test, which are surveyed in [20]. One of the most common communications test approaches is utilizing Built-In Self-Test (BIST). This mechanism is considered as cost-effective and prevalent for a variety of reasons such as external test equipment unnecessity, test performance with circuit speed, high testability, and offline and online test performance [21]. In this structure, Test Pattern Generator (TPG) on the one hand of the unidirectional channel generates test patterns and applies to it; and on the other hand, Test Response Analyzer (TRA) receives and analyzes the test results. To test bi-directional channels between the routers of R_i and R_j, (R_i, R_j), therefore, the two units are required to be embedded both in R_i router and R_j router [22]. Moreover, to test the bi-directional channel between the router and Network Adaptor (NA), (NA_i, R_i), both units can be located in NA [23]. With an increase in NoC dimension, however, hardware redundancy increases substantially.

All things considered, some fault tolerant approaches utilize additional hardware to save up the fault information. In some other approaches, additionally, the system consumes excessive time to convey the fault information. Furthermore, a research gap exists between test mechanisms and fault tolerant methodologies. The methodologies

E-mail address: B.aghaei@iaut.ac.ir.

http://dx.doi.org/10.1016/j.microrel.2017.07.010
0026-2714/

proposed to increase fault tolerance, simply put, have not completely elucidated the test mechanism as well as how they track the faulty elements; or, the idea how the test mechanisms employ fault tolerant and debugging methods to keep a record of fault information has not been explicated as well. This paper aims to propose a methodology that simultaneously searches, detects, and locates the faults in NoC communication channels. Each router, in this methodology, is capable of detecting and locating the faults on the connected channels through comparing the entering packets. The contributions made by the proposed approach are as follows: 1) Presenting a high fault coverage test methodology for detection and location short faults in NoC communication channels, 2) Providing a BIST-based approach with minimum time and hardware costs.

This paper is organized as follows: Section 2 reviews recent related works. Section 3 explicates short faults models. The proposed approach is presented with detailed elucidation in Section 4. Investigating fault detection and location capability of proposed approach is presented in Section 5 and its scalability in Section 6. Hardware considerations and test mechanism timing are discussed in Sections 7 and 8, respectively. The paper, eventually, ends with presenting the simulation results and comparisons in Section 9 and the conclusions and future works in Section 10.

2. Related works

The test of an NoC-based SoC for detecting manufacturing defects and lifetime is usually divided into two parts: the test of the IP cores and the test of the communication infrastructure. In the test of the cores, NoC structure is typically used as Test Access Mechanism (TAM) to reduce the test overhead [24,11,25,9,26,27,10]. The test of the communication infrastructure encompasses routers test and communication channels. A bulk of investigations [19,13,16,18,15,17,14] has been conducted to test the routers. The test of NoC communications has borrowed some of its concepts from previous researches on System on Board (SoB). The instances of this can be observed in such permanent faults as Stuck at fault, shorts, opens, and delay [28–31] as well as impermanent faults such as crosstalk [32].

Raik et al. [33] have proposed an external test method which is capable of functionally testing the switches and the channels to detect delay faults, opens, and shorts. Grecu et al. [22] propose a BIST methodology for at-speed testing the channels of the communication platform among the routers. The proposed methodology aims at targeting crosstalk faults assuming the MAF fault model [32] and short faults can be detected as well. The test patterns are located in the payload packets and then are transmitted to the channels being tested. The authors have therefore managed to reduce the test time using test parallelism. Petersen et al. [34] developed a functional and scalable online-structural methodology for a two-dimensional mesh which works with system speed. In this method, similarly, a BIST structure at chip initialization tests the communication channels among the routers to detect the physical faults. To the best of our knowledge, the paper by Cota et al. [23] is one of the most thorough works in the communications test in which a functional test strategy has been proposed to detect shorts in the data links, handshake in an NoC channel with a grid topology. The researchers embedded the TPG and TRA in the NA and then detected the network shorts through generating test packets, transmitting them to neighbors, and analyzing the results. In this method, although the hardware overload is diminished, the faults are not located. Herve et al. [35], having understood this, could manage to detect 93% of the shorts in the communication channels following their development of the previous method and proposing a fault detection method. This detection requires 16 times of configuration and 5 rounds of test cost in a 5×5 grid network. Their proposed method, hence, faced drawbacks in the fault location. Concatto et al. [36], similarly, employed this methodology for a mesh network. The method suggested encompasses the detection and diagnosis of shorts in the communication channels through employing a BIST as well as activating an alternative path for the faulty channels. Herve et al. in their subsequent work [37] integrated the functional test presented in their former paper with the routers test. Strano et al. [38] proposed a BIST and self-diagnosis structure for stuck at fault test. Kakoee et al. [39] proposed an on-line test mechanism in which each router with the neighboring routers' assistance was capable of detecting all stuck at faults and shorts only on the channels among the routers. Ghofrani et al. [7] assert that they have proposed a comprehensive and cost-effective solution for the detection and diagnosis of permanent on-line faults on channels. Employing an error syndrome collection and flit/packet counting technique, they are capable of detecting the faults on the control and data lines. Kakoee et al. [40] in another work proposed a detection and diagnosis structure for delay, shorts, and stuck at faults in the NA and the communication channels. Bhowmik et al. in their works [41–43], recently, suggested an on-line test structure for the detection of shorts in the communication channels. Their works are mainly characterized by a high level simulation that is able to assess the effect of number of test rounds upon such network efficiency parameters as power consumed, delay, and throughput. To the best of our knowledge, the works conducted by [39,7] can be regarded as more comprehensive investigations on faults location in the NoC channels. These papers, however, have not addressed the fault detection in the channels between the router-NA. Their proposed methodology, on the other hand, greatly increases the system hardware overhead and also various configurations are required for the complete implementation of the approach. Other papers, similarly, have not addressed how the test results are employed for faults location. In two later works [44,45], we proposed a new online and offline search, fault detection, and fault location approach for short faults in NoC communication channels. In continue last our works, in this paper, we aim to optimize fault coverage of test strategy by modifying the PCM unit.

3. Fault space model

Given the fact that NoC is composed of routers, communication channels, and NAs, fault can take place in each of them. In this paper, the focus is upon the shorts occurring in the communication channels with a moderate view because the assumption that all NoC channels be faulty simultaneously does not appear realistic [23]. Short fault refers to a situation in which the number of k wires is connected to each other within a single channel. The fault can be observed in both communication channels of Router-to-Router (Ri, Rj) and Router-to-NA (Ri, NAi) in two directions. Short faults are twofold: OR-short and AND-short [42]. Both faults categories influence the network efficiency. The present paper concentrates upon intra channels short faults. Fig. 1 illustrates short faults in intra communication channel (Ri, Rj).

In Fig. 1, f_{sab} is used to define a short fault between the two l_b and l_a wires. The number of N_S short faults on the channel is obtained with the n number of wires by the following equation [43]:

$$Ns = \sum_{k=2}^{n} \frac{n!}{k!(n-k)!} \tag{1}$$

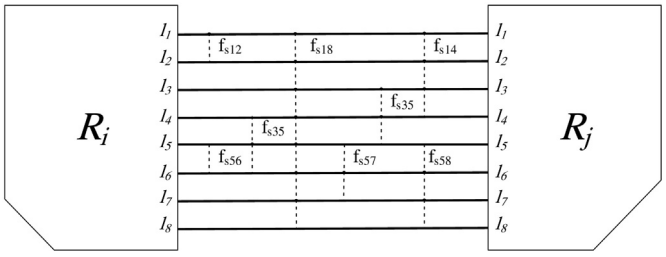

Fig. 1. Short faults in the channel (R_i, R_j).

Please cite this article as: B. Aghaei, A high fault coverage test approach for communication channels in network on chip, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.07.010