Microelectronics Reliability 78 (2017) 38–45

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Review paper

Soft error rate comparison of 6T and 8T SRAM ICs using mono-energetic proton and neutron irradiation sources

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ARTICLE INFO

Article history:
Received 30 January 2017
Received in revised form 28 July 2017
Accepted 28 July 2017
Available online xxxx

Keywords:
Soft errors
Single event effects
Single Event Upset
Radiation effects
SRAM
Neutrons

ABSTRACT

We present experimental results of soft errors produced by proton and neutron irradiation of minimum-size six-transistors (6T) and eight-transistors (8T) bit-cells SRAM memories produced with 65 nm CMOS technology using an 18 MeV proton beam and a neutron beam of 4.3–8.5 MeV. All experiments have been carried out at the National Center of Accelerators (CNA) in Seville, Spain. Similar soft error rate levels have been observed for both cell designs despite the larger area occupied by the 8T cells, although the trend for multiple events has been higher in 6T.

Contents

1. Introduction

The design and implementation of faster, more complex and compact systems, has been greatly benefited by the development of modern microelectronic nanometer technologies [1]. This progress has been possible thanks to the decrease of supply voltage and aggressive

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http://dx.doi.org/10.1016/j.microrel.2017.07.093
0026-2714/

technology scaling, which as a collateral effect has led to new mechanisms contributing to device reliability issues. In this way, ionizing radiation effects are not a specific problem exclusively related to space or avionic applications anymore and have become a major concern for reliability and dependability of emerging electronic devices [2].

Alpha particles, neutrons, protons, heavy ions and other ionizing particles may interact with solid-state devices impacting their behavior [3]. Particle interactions with silicon lattice are capable of generating electron–hole pairs in the circuit substrate. The drift and diffusion of the resulting charge carriers can produce a disturbing transient current when they are collected at a circuit node. If the collecting node is part of a combinational logic block, a Single Event Transient (SET) is generated, while if the part affected is an internal node of a memory cell, the current pulse may change its logic state leading to a corrupted data bit, causing a Single Event Upset (SEU) or soft error.

This effect only occurs when the collected charge surpasses a given threshold value (critical charge) that depends on the fabrication technology, the bit-cell design at circuit level, the layout and the transient characteristic of the induced current [4]. SEUs can be further categorized as SBU (Single Bit Upset) when only the state of a single register is affected or as MBU (Multiple Bit Upset) when more than one register is modified by the event. Note that a SET within a combinational block can be propagated through a number of combinational logic gates and may finally induce a soft error if caught by a register. The SEU itself is not considered to permanently damage the affected device since it operates normally after the disturbance.

Currently, many systems-on-chip designs use a major part of the die for embedded static memory. When one or more memory cells are corrupted by radiation, stored data may be irreparably corrupted or lost. For these reasons, it becomes critical to analyze the impact of soft error in the overall system error rate of static memories [5].

With smaller device size and more aggressive design rules related to nanometer technologies, the standard six transistors cell (6T) shown in Fig. 1 has become more sensitive to device variations and more prone to functional failures than before [5]. SRAM cells must retain their value during a read access and change it during write operations. Cell stability during read mode is enhanced by weakening the access pass-transistors and strengthening the inverters of the internal latch, however, the opposite is desired to improve writing ability, resulting in conflicting constraints on transistor sizing of 6T cells [6]. Alternative cell structures have been proposed to overcome the limitations of 6T cells by separating read and write modes at the cost of increasing the transistor count to 8T [7], 9T [8] and 10T [9] cells. The 8T cell (Fig. 1) allows reusing traditional SRAM design techniques and is being adopted as an alternative to the 6T cell in industrial designs. Such replacement is especially attractive when several supply voltages levels are required to achieve high performance during the normal mode while minimizing power consumption during low voltage modes [7].

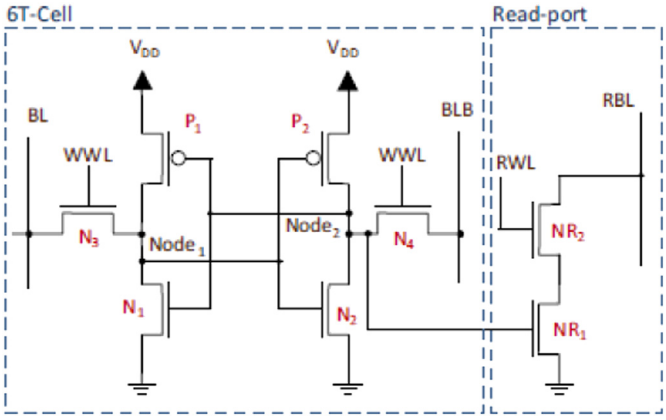

Fig. 1. Schematic of an 8T SRAM cell. It consists of a conventional 6T SRAM cell, formed by pull-down transistors N_1 and N_2, pull-up transistors P_1 and P_2, access transistors N_3, N_4 completed with an additional read port formed by transistors NR_1 and NR_2.

However, limited experimental data about the effect of radiation on the behavior of 8T cells is available. The comparative studies between 6T and 8T memory cells are usually based on analyzing their respective critical charges, Q_{crit}, calculated from electrical simulation, although it has been shown that Q_{crit} alone is not enough to quantify the device soft error rate (SER) [10]. This is because the response to radiation is also influenced by the cross-section and charge collection efficiency of circuit sensitive nodes, being aspects not usually considered in critical charge simulations, as experimentally corroborated in [10]. The aim of this work is to complement these previous works based on Q_{crit} analysis and alpha induced soft errors, by reporting experimental data on neutron (1–10 MeV range) and proton induced SER in minimum sized 6T and 8T cells.

2. Soft error sources

High energy neutrons and thermal neutrons in the terrestrial cosmic ray, and alpha particles from the decay of radioactive isotopes present as impurities in encapsulation and component materials are considered to be the three major causes of soft errors in microelectronic devices [3].

In terrestrial environments (i.e. from sea level to 10,000 ft), neutrons are the dominant cosmic ray by-products that cause soft errors [11]. High-energy neutron spectrum starts at ~1 MeV and extends up to almost 10 GeV. High-energy neutrons can lose energy by scattering with materials in the environment and ultimately reach the thermal equilibrium energy, becoming thermal neutrons (~25 meV) [4]. The typical shape of the energy differential spectrum in isolethargic (logarithmic) units at ground level is shown in Fig. 4 of [4]. As a good approximation, between the evaporation peak (~1 MeV) and the thermal peak, the energy differential spectrum dn/dE can be considered to be proportional to 1/E.

Neutrons are not directly ionizing particles, however over an energy threshold they can interact with the ^{28}Si atoms and other elements used by the microelectronic technology, creating secondary ionizing particles (spallation), for silicon target, the created ion species range from hydrogen to phosphorus [12]. These secondary particles can be generated anywhere in the semiconductor material and emitted in any direction. Some of these reactions occur above energy thresholds of few MeVs, such as $^{28}Si(n,p)^{28}Al$ with a 4 MeV threshold and $^{28}Si(n,\alpha)\ ^{25}Mg$ with 2.7 MeV threshold.

The thermal part of the spectrum is capable of inducing soft errors in ICs because of the very large reaction cross section of thermal neutrons with ^{10}B, an isotope that was commonly found in many IC processes as a substrate dopant and in the glass passivation layers. The most probable result of the interaction of a thermal neutron with ^{10}B is a 1.87 MeV alpha particle and 0.84 MeV ^{7}Li particles along with a 0.48 MeV photon [13]. Both α-particle and lithium nucleus release enough energy to cause the cell upset. With the suppression of BPSG layers in recent fabrication technologies, neutron induced SEUs in SRAM based systems are now mostly attributed to high-energy neutrons [4].

It has been recently reported that below the 0.25 μm CMOS IC technology node, bulk technologies exhibit a relatively high sensitivity to neutrons between 4 and 6 MeV, which is explained by the contribution of alpha particles coming from (n,α) reactions. Recent SRAM technologies (below 0.18 μm) exhibit a significant SEU sensitivity to neutron energies as low as 4 MeV [14], while the 65 and 90 nm nodes have shown SETs at 1 MeV [15]. Taking into account the amount of neutrons in the

Table 1
SRAM features.

	Cell architecture	Block size	Cell area (μm^2)
Memory 1	6T	256 × 64	1.01
Memory 2	8T	256 × 64	1.39