Microelectronics Reliability 78 (2017) 190–196

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Towards high-sensitive built-in current sensors enabling detection of radiation-induced soft errors

Raphael de Oliveira Rocha [a], Frank Sill Torres [a,*], Rodrigo Possamai Bastos [b]

[a] Federal University of Minas Gerais, Belo Horizonte, Brazil
[b] Univ. Grenoble Alpes, CNRS, TIMA, Grenoble, France

ARTICLE INFO

Article history:
Received 16 December 2016
Received in revised form 4 July 2017
Accepted 21 August 2017
Available online xxxx

Keywords:
Built-in Current Sensors
Soft errors
Transient faults
Reliability

ABSTRACT

Soft error resilience is an increasingly important requirement of integrated circuits realized in CMOS nanometer technologies. Among the several approaches, Bulk Built-in Current Sensors (BBICS) offer a promising solution able to detect particle strikes immediately after its occurrence. Principal challenges for its wide application in common designs are area costs and robustness, both directly related to the sensor's sensitivity. Following this requirement, this work presents strategies enabling the design of high-sensitive BBICS. In detail, we are proposing three approaches based on gate voltage control, body biasing, and stack forcing that can be integrated in all *state-of-the-art* BBICS architectures. In order to verify the feasibility of this approaches, the proposed techniques have been integrated in a modular BBICS realized in a commercial 65 nm technology. Simulation results indicate an increase of the detection sensitivity by up to factor 6, leading to 17% area overhead, response times around 1 ns, a negligible power penalty, and high robustness against wide variations of temperature and process parameters.

1. Introduction

CMOS remains the dominating technology for integrated circuits, mainly due to its miniaturization capability and high integrability. However, the continuously reduction of technology sizes results in designs that are susceptible to several fault sources like parameter variations [1], oxide breakdown [2], and radiation [3]. In case of the latter, energetic particles inject electrical charge into sensitive regions of the semiconductor devices, creating transient currents that can result in soft errors. For years, researches on radiation-induced soft errors concentrated mainly on memories and application intended for avionics and aerospace environment. However, as current technologies reached nanometer scale, soft error resilience is also required for applications on ground level as well as the combinational parts of the circuits. Several concurrent error detection and/or correction techniques have been presented to circumvent the effects of soft errors. This includes the application of multiple clocking schemes [4], checker-based arithmetic units [5], and selective redundancy [6]. In contrast to gate and system level techniques, Bulk Built-in Current Sensors (BBICS) are a promising approach on transistor level, which enables the detection of radiation-induced particle strikes immediately after its occurrence [7–10]. BBICS offer fast error detection and low cost in terms of power. On the downside, BBICS design is a challenging task, as these sensors tend to be prone to parameter and temperature variations and/or require a considerable amount of area [11–13]. Previous works introduced several different kinds of BBICS architectures, including the single BBICS [14], the modular BBICS [15,16], the dynamic BBICS [17], a low-leakage BBICS [18], as well as an architecture based on transistors with different threshold voltages [19]. Despite the diversity of BBICS architectures, there is still a demand for further improvements. Principal requirements are reduction of area costs and robustness.

This work presents several new concepts leading to considerable enhanced sensitivity, and thus, to notably improved area costs, response time, and robustness. The proposed techniques can be employed by all reported BBICS architectures turning the results of this work into an important step towards the consolidation of the BBICS approach.

The rest of the paper is organized as follows. Section 2 introduces basic information and the BBICS method, while Section 3 details the new strategies. Section 4 is related to simulation results. Finally, Section 5 draws the conclusion.

2. Preliminaries

This section discusses the generation of transient faults induced by radiation on integrated circuits and introduces the BBICS approach.

* Corresponding author.
E-mail addresses: franksill@ufmg.br (F. Sill Torres), rodrigo.bastos@univ-grenoble-alpes.fr (R.P. Bastos).

http://dx.doi.org/10.1016/j.microrel.2017.08.015
0026-2714/

2.1. Transient faults and soft errors

Unintentional transient signal variations in integrated circuits are defined as transient faults. A transient fault can turn into a soft error when it propagates to the input of a sampling element or affects directly a node within the sampling element, for example a latch or flip-flop.

There are several sources for transient faults like cross-talk, ground bounce, or radiation-induced energetic particles [20]. The latter are critical for reversed-biased p-n junctions, as it is the case for drain or source regions of transistors in cut-off state. In the event of a particle strike, the electron-hole pair track formed in the path of the energetic particle affects the electrical field in the depletion region to shortly adopt the shape of a funnel towards the substrate [21]. This starts the so-called carrier collection that is observed as transient voltage on the affected node. The subsequent phase of carrier collection is defined by a slower phenomenon in which carriers are conducted through the depletion region due to diffusion. The corresponding current pulse is traditionally modeled by a double-exponential function I_{coll} by following equation [22]:

$$I_{coll}(t) = \frac{Q_{coll}}{t_f - t_r}\left(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}\right) \quad (1)$$

Hereby, Q_{coll} is the total collected charge, and t_r and t_f represent the time constants for the funnel collection and he second phase of carrier collection.

2.2. BBICS detecting transient faults

The idea behind BBICS is to monitor anomalous currents in the transistor bulk in case of a particle strike [7,12]. Consequently, it enables the detection of radiation-induced currents that might lead to soft errors.

The principal idea of BBICS shall be introduced with the aid of the modular BBICS (mBBICS) reported in [15]. It consists of functional blocks named as head and tail (see Fig. 1). The head circuits are connected to the bulk of the monitored devices, *i.e.*, the Block Under Test (BUT) in Fig. 1, and act as sensing elements. The outputs of several heads (wire $head_{NMOS}$) are latched by the tail circuit. As most of *state-of-the-art* BBICS, the mBBICS approach comprises a NMOS type able to detect transient faults in NMOS devices and a complementary PMOS version.

Fig. 1 illustrates an NMOS-mBBICS in which the gate of transistor Nh1 is connected to VDD and the drain to the NMOS bulk of the monitored transistors in the BUT. In normal operation, the drain of Nh1 acts as a virtual GND, while the head output (*i.e.*, drain of Nh2) is at VDD level. In case of a particle strike, the fault current in the bulk is conducted through Nh1, resulting in a voltage drop over Nh1 that increases the gate voltage of Nh2. If this voltage exceeds the threshold voltage $v_{th,Nh2}$ of Nh2, this device is switched on and the signal $head_{NMOS}$ is pulled down, leading the tail circuit to latch this signal and set an error flag. The circuit remains in this logic state until the reset transistor Pt3 is activated, turning the sensor ready for another detection [15].

The PMOS-mBBICS, which permits the detection of transient faults in PMOS devices, has a complementary behavior and structure and is omitted herein for the sake of simplicity.

The sensitivity of a BBICS relates to the amplitude of a radiation-induced bulk current that can be detected. The amplitude of this current correlates with the collected charge and the capacitive load of the sensor's input [23]. The latter is directly related to the number of monitored devices. Hence, the higher the BBICS's sensitivity the greater the number of devices a single BBICS can monitor and, consequently, the lower the area penalty [24].

Note that the processing of the generated error flag in case of a transient fault is realized on higher abstraction layers and is not discussed in this work. Further information can be found in [25–29].

3. Strategies for improving BBICS

This section presents the strategies for improving the sensitivity of BBICS architectures, leading to enhanced response time, area costs, and robustness. All techniques are applied exemplarily for the mBBICS architecture. Nevertheless, we would like to emphasize the universality of the approaches for different types of BBICS architectures.

For the sake of simplicity, the discussions relate solely to the NMOS version, but it can be carried over directly to the complementary PMOS type.

3.1. Adjustable gate voltage on sensing transistor

A common element of BBICS architectures is the sensing device that converts the bulk current into a voltage signal [12,17,18,30]. In case of the mBBICS, transistor Nh1 is this element (see Fig. 1 and Section 2.2). At the onset of a particle strike and a resulting bulk current, the voltage drop at the drain of Nh1 must be sufficient to activate Nh2, and thus switching the signal $head_{NMOS}$. It is, therefore, desired that the current through Nh1 results into a high voltage drop over Nh1. On the other side, it has to be assured that the bulk voltage must be kept at GND level in fault-free operation mode. Previous BBICS [8,11,15,18] achieved these goals by using a transistor with small W/L ratio that operates in linear mode, *i.e.*, a gate-source voltage equal to VDD. Consequently, the sensor sensitivity can be calibrated by adjusting the gate length of

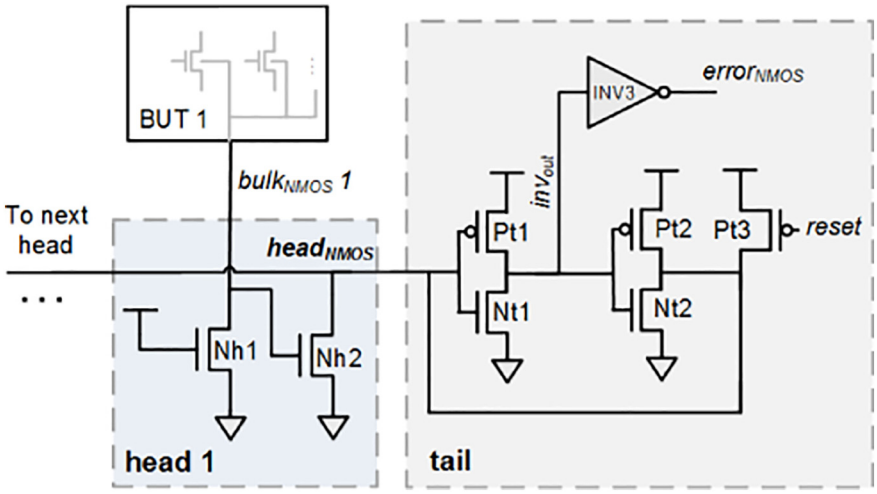

Fig. 1. mBBICS architecture (head + tail, NMOS type) able to detect transient faults in the monitored blocks defined as BUT.