Interface traps effect on the charge transport mechanisms in metal oxide semiconductor structures based on silicon nanocrystals

S. Chatbouri [a],*, M. Troudi [a], A. Kalboussi [a], A. Souifi [b]

[a] Laboratoire de Micro'électronique et Instrumentation (LR13ES12), Faculté des Sciences de Monastir, Avenue de l'environnement, Université de Monastir, 5019 Monastir, Tunisia
[b] Institut des Nanotechnologies de Lyon - site INSA de Lyon, UMR CNRS 5270, Bât. Blaise Pascal, 7 Avenue Jean Capelle, 69621 Villeurbanne Cedex, France

ARTICLE INFO

ABSTRACT

The transport phenomena in Metal-Oxide-Semiconductor (MOS) structures having silicon nanocrystals (Si-NCs) inside the dielectric layer has been investigated by high frequency Capacitance-Voltage (C-V) method and the Deep-Level Transient Spectroscopy (DLTS). For the reference samples without Si-NCs, we observe a slow electron trap for a large temperature range, which is probably a response of a series electron traps having a very close energy levels. A clear series of electron traps are evidenced in DLTS spectrum for MOS samples with Si-NCs. Their activation energies are comprised between 0.28 eV and 0.45 eV. Moreover, we observe in this DLTS spectrum, a single peak that appears at low temperature which we attributed to Si-NCs response. In MOS structure without Si-NCs, the conduction mechanism is dominated by the thermionic fast emission/capture of charge carriers from the highly doped polysilicon layer to Si-substrate through interface trap-states. However, at low temperature, the tunneling of charge carriers from highly Poly-Si to Si-substrate trough the trapping/detrapping mechanism in the Si-NCs contributed to the conduction mechanism for MOS with Si-NCs. These results are helpful to understand the principle of charge transport of MOS structures having a Si-NCs in the $SiO_{x\,=\,1.5}$ oxide matrix.

1. Introduction

The Metal-Oxide-Semiconductor (MOS) structures having nanocrytals (NCs) embedded in their oxide layer (smart non-volatile memory devices [1–6], third generation solar cells [7] and single-electron devices [8]) have received much attention as promising candidates to replace conventional polycrystalline silicon or silicon nitride non-volatile memories for future high capacity and low power consuming memory devices. In this structure we see that there are likely traps present at the NC - matrix interface, at the Si/SiO_2 interface. The NCs (Si, Ge …), presence in tunneling layer contributes to either directly to the memory effect or affects the charge trapping dynamics of the NC's. The NC's charging and discharging are widely supposed to take place by direct tunneling of charge carriers from/to the free carrier reservoir in the semiconductor substrate. So, the charge emission from NCs cannot be characterized by direct tunneling but rather by a trap assisted tunneling mechanism, with the Si/SiO_2 interface states playing a key role as transfer nodes [9–11]. The energy distribution, the density of traps and capture kinetics of the interface and oxide traps are crucial for the future device applications. To obtain those information deep level transient spectroscopy (DLTS) could be used. Then, the DLTS technique is used to analysis the trap states in the semiconductors [12], and recently it has been applied

in studying the semiconductors quantum dots (QD) [13]. In order to apply DLTS for studying MOS structures containing the nanocrystals it is necessary to obtain and analyze DLTS results on clean MOS structures (i.e. without nanocrystals). This will be enabling to separate DLTS signals coming from Si/SiO_2 interface and Si nanocrystals.

In this work, we confirmed the contribution of interface traps in the DLTS response of a MOS with and without Si-NCs. This contribution is marked on series of electron traps with too tight activation energies. This quantum of electron traps, assured the thermionic transition from conduction band of Poly-Si to conduction band of Si substrate. The DLTS response of Si-NC as a single point deep level defect in the oxide is confirmed also. So, the tunnel emission dot to dot at low temperatures will be an important factor to understand the principle of charge transport in MOS structures having a Si-NCs in the $SiO_{x\,=\,1.5}$ oxide matrix.

2. Experimental details

The MOS structures were developed in the Sherbrooke University combining nanolithography and reactive ion etching (RIE) process. The schematic cross-sectional structure of our device discussed in this paper is shown in Fig. 1(a). Over a silicon (N-type) substrate, a non-stoichiometric oxide layer $SiO_{x\,=\,1,\,5}$ is deposited by Low Pressure Chemical Vapor Deposition (LPCVD) with two thicknesses: 5 and 10 nm (The fabrication and insulation of the oxide layer rich in silicon (SRO) is performed at CEA-LETI Grenoble). Then the layer is annealed

* Corresponding author.
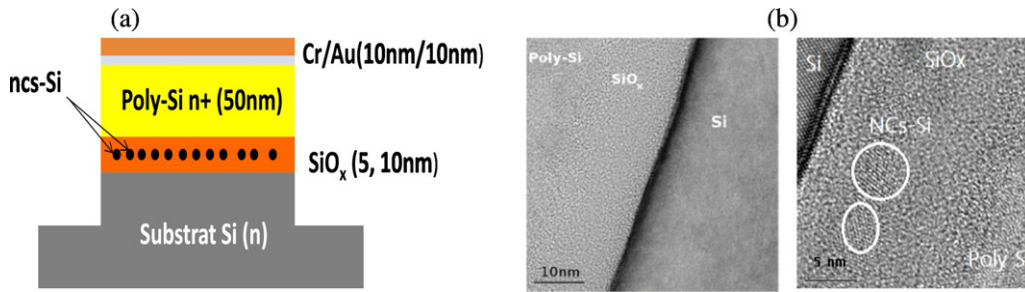E-mail address: samir.chatbouri@yahoo.com (S. Chatbouri).

Fig. 1. (a): The schematic cross-sectional of MOS silicon nanocrystals structure, (b): TEM micrograph of MOS structures with and without silicon nanocrystals.

of demixing for 3 min 30 s at 1000 °C in order to form silicon nanocrystals. A second annealing in oxygen at 1000 °C will be affected with a period of 5, 10 or 30 min. This annealing oxidizer allows the passivation of the nanocrystals surface. Finally, a high doped layer of polysilicon (with a doping density $N_{Poly-Si} = 2 \times 10^{20}$ cm^{-3}) is deposited by LPCVD on SiO_x layer. The nanocrystals are formed by annealing the SRO in nitrogen environment. After the annealing, Si-dots appear in thick and thin layers. The oxide is composed of silicon nanocrystals (Si-NCs) embedded in $SiO_{x = 1.5}$ layer. The thick $SiO_{x = 1.5}$ layer presents spherical silicon crystallites with an average size around 5 nm extracted from transmission electron microscopy (TEM) measurements (Fig. 1(b)). The Si-NCs density is about ~1.6×10^{-11} cm^{-2}. A second annealing step in oxygen was also performed. We used e-beam lithography and dry etching to obtain the vertical structures. 200×200 μm^2 active area detectors are finally obtained. The electrical insulation is provided by planar photosensitive resist: it was spun and then etched back by O_2 plasma. Then a semi-transparent contacts Cr/Au (10 nm/10 nm) were formed on the polysilicon through photolithography and lifting of a bi-layer LOR 5A/S1813. They were then used as etching masks RIE to isolate the capacitors. The substrate is used for electrical continuity. Table 1 shows the layers structures of MOS of two samples (A) and (B). Sample (A) has a 5 nm thick $SiO_{x = 1.5 \, layer}$ without Si-NCs (Reference), whereas sample (B) has a 10 nm thick $SiO_{x = 1.5}$ and indicate the presence of Si-NCs within the oxide layer.

The C-V and DLTS measurements were performed by a capacitance meter at a frequency of 1 MHz (model 410 C-V Plotter) with high resolution mode. To vary the filling pulse width, a pulse generator (Philips PM 5771) was used. The temperature measurement was varied in the range of 20–325 K by using a closed-cycle liquid helium cryostat with a Lakeshore 330 auto-tuning temperature controller. For this system, the DLTS spectra will be made at a temperature where the locking frequency, f, was related to the emission rate by $e_n = 2.13$ f [14].

3. Results and discussions

Fig. 2(a and c) shows the C-V measurements observed in MOS structure; a: reference sample: without Si-NCs, b: with Si-NCs: MOS-NCs. First, we can see the total absence of hysteresis in the reference sample which means that there is no accumulated charge, so there is no Si-NCs at all the 5 nm $SiO_{x = 1.5}$ layer. A clockwise hysteresis was observed for MOS-NCs, this hysteresis should be attributed to electron trapping into the Si-NCs or/and the interface of the nanocrystals dots, and not to

defects in the oxide matrix or at the Si substrate/tunnel oxide interface [15].

The density of traps and the information regarding the energy distribution are crucial for the future device MOS applications. To obtain this information, deep level transient spectroscopy (DLTS) could be used [12,13].

A DLTS measurements have been carried out in temperature range from 50 to 320 K by varying the applied gate voltage from -2 V to 0.5 V for windows ($e_n = 426$ s^{-1}) and a filling pulse time of 0.5 ms (Fig. 2(b: reference sample, and d: the MOS-NCs)).

The DLTS is a well-established technique which is commonly used in studying the trap states in the semiconductors [16], recently it has been applied in studying the semiconductor based nanocrystals [17]. In Fig. 2(b), we have observed a one positive signal for a large range temperature (120 K–300 K) in the DLTS spectrum for the MOS structure without Si-NCs. This signal is probably a DLTS-response of a series electron traps with energy levels too close. This hypothesis can be enhanced by the DLTS-response for a Si-NCs-MOS (Fig. 2(d)), where we can see clearly the separation on a series of multi-electron trap. Moreover, one positive signal corresponding to an electron trap has appeared for low temperature (70 K).

The principle of the DLTS technique consists in the analysis of the emission and capture assessed traps to variations in capacitance of a p-n junction or a Schlocky diode. This is achieved by charging and discharging the traps repetitively, with a positive and/or negative polarization voltage applied to the sample. The curvature of the energy bands of semiconductor varied with the applied voltage, so a trap charge state will be dependent of the polarization and the capacity of the space charge region will be affected. During the pulse charging, the space charge zone decreases and the traps that lie below the Fermi level can be filled. In order to explain the origin physical of these signals, we need information on space zone depleted by the voltage bias, so the first step is the calculation of space charge zone extension 'w'. In our case we assume that the deep defect concentration is uniform with the space charge zone extension 'w' as the following Eq. (1) demonstrates [18]:

$$w = \sqrt{\frac{2\varepsilon}{q(N_d + N_{T\partial}^{+})}\left(V_{bi} - V_r - \frac{kT}{q}\right)} \quad (1)$$

where N_d Doping concentration, N^+_T: deep defects concentration, V_{bi}: intrinsic potential, V_r: applied potential.

Our structures are doped N^+ following densities ($N_{Si} = 6 \times 10^{17}$ cm^{-3} and $N_{Poly-Si} = 2 \times 10^{20}$ cm^{-3}), which give a value of 'w' about 238 μm, so we can assume that the totality of the structure is scanned by the potential.

At low temperature (about 70 K), we can see that the electron trap appears only for the MOS with Si-NCs, so it is likely that a silicon nanocrystals DLTS response (Si-NCs DLTS-response) have a high size dispersion of quantum dots which are considered as storage nodes. The thermally stimulated process is involved in the electron capture (hole emission) in the Si-NCs. In this case the interface state may play

Table 1
MOS structures.

Sample (A)	Sample (B)
$SiO_{x = 1.5}$ (5 nm)	$SiO_{x = 1.5}$ (10 nm)
1000 °C/3 min 30 s/N_2	1000 °C/3 min 30 s/N_2
1000 °C/5 min/O_2	1000 °C/5 min/O_2
Poly Si N^+ 50 nm	Poly Si N^+ 50 nm
Substrat Si type N	Substrat Si type N