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Simulation comparison of InGaP/GaAs HBT thermal performance in wire-bonding and flip-chip technologies

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ABSTRACT

This paper presents an extensive numerical analysis of the thermal behavior of InGaP/GaAs HBTs for handset applications in a laminate (package) environment. Both wire-bonding and flip-chip technologies are examined. The combination between an accurate, yet fast, simulation capability and the Design of Experiments technique is employed to quantify the impact of all the key technology parameters and explore a wide range of operating conditions.

1. Introduction

Gallium arsenide (GaAs) heterojunction bipolar transistors (HBTs) are the dominant technology for handset power amplifier design by virtue of features like high power density, cut-off frequency, and efficiency [1]. Unfortunately, these devices are plagued by electrothermal effects due to mesa isolation and low thermal conductivity of GaAs (one third of that of silicon), which–combined with high operating currents–can lead to performance degradation, long-term reliability issues, and also sudden device failure (as an example, multifinger transistors biased with a constant base current may suffer from current focusing, which can be performance-limiting due to the *gain collapse* or even destructive [2–6]). Since the late eighties, the literature has been populated by papers centered on the thermal behavior of single- and multi-finger GaAs HBTs with the aim of achieving a thermal-aware design (e.g., [2–27]). Several studies have been focused on the metallization due to the relevant role played by the upward heat flow [11] (the poor GaAs conductivity hinders the heat transfer to the backside); in particular, most of them have proposed and/or analyzed solutions based on thermal shunts [8,12,16–20,23,25]. Other works dealing with multi-finger transistors have promoted emitter or base ballasting [15,19,27], and nonuniform finger spacing or length for an assigned die and emitter area [22,27]. Some papers have also investigated the beneficial effect of a more thermally conductive and/or shorter path from the heat dissipation region and the sink, which can be obtained with flip-chip (FC) packaging [9,10,14,16,18] or alternative solutions based on thermal vias [13,25]. Little attention was instead paid to other technology features like the specifics of the emitter stack (with the exception of [18]), which cannot be disregarded since in modern InGaP/GaAs HBTs the ternary InGaAs and InGaP emitter layers suffer from thermal conductivities even poorer than GaAs (and thus thermal shunt solutions are less effective); moreover, since designs are moving to FC, the thermal impact of the emitter is expected to be amplified since the heat propagates through it to the sink. In addition, no studies have been published that report an exhaustive thermal comparison between the conventional wire-bonding (WB) technology–still largely adopted due to its flexibility, existing infrastructure, and low cost–and the FC assembly, which benefits from a smaller package size and aims to boost the performance.

In [28], a first attempt was made to fill some of the above gaps by investigating the influence of emitter stack, metallization, and emitter layout upon the thermal behavior of simple unpackaged single-emitter InGaP/GaAs HBTs; an *accurate* and *efficient* analysis was conducted by

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combining (i) a simulation strategy relying on the finite-element method (FEM) aided by an *in-house* script for automatic geometry/mesh generation and solution, and (ii) the Design of Experiments (DOE) to identify the individual and concurrent impact of many parameters with a minimized number of simulations. The approach was then applied to the practical case of four-emitter HBTs in WB technology in [29], where the laminate (package) design was also examined; although usually ignored in the literature, the laminate must be accounted for since it represents how the HBT IC technology is actually used in today's high volume commercial mobile communication products. In addition, the analysis covered the impact of temperature of laminate backside and dissipated power.

This paper extends [28,29] by (i) accounting for the thermal conductivity degradation of GaAs in the ion-implanted isolation regions in both WB and FC solutions, and including the glue (epoxy) layer between GaAs substrate and laminate in WB packaging; (ii) providing more details on the simulation approach and DOE procedure, (iii) examining–for the first time–the thermal influence of all HBT features in FC assembly, namely, emitter architecture, metal layers, die-pillars connection, pillar structure, and laminate design, and (iv) comparing the thermal performance of FC and WB. The objective is to offer exhaustive information on the proper choices of all key parameters to GaAs HBT designers, as well as guidance to modeling, reliability, and packaging engineers, also including some often-overlooked details and accounting for the uncertainties on various relevant thermal conductivities. This can be helpful to mitigate the thermal impact on circuit performance, which is a great concern especially for WLAN (e.g., [30,31]).

The paper is arranged as follows. Section 2 illustrates the transistors under analysis, as well as the details of the WB and FC configurations. In Section 3, the numerical simulation strategy is described. The DOE procedure is outlined in Section 4. Section 5 presents and discusses the results. Conclusions are then drawn in Section 6.

2. Devices under test

The devices under test (DUTs), the schematic cross-section of which is represented in Fig. 1a, are typical mesa-isolated NPN HBTs with four $2 \times 20.5\ \mu m^2$ emitters, manufactured by Qorvo using an HBT-only process (e.g., [32]). The emitter stack is composed by (from the top): (1) a cap with an $In_{0.5}Ga_{0.5}As$ layer (used to minimize the contact resistance with Au) and a grading $In_xGa_{1-x}As$ layer with x decreasing from 0.5 to 0 (to ensure a good continuity from the $In_{0.5}Ga_{0.5}As$ to the GaAs lattices); (2) a GaAs layer (as a set-back used for easier processing); (3) a deep $In_{0.49}Ga_{0.51}P$ layer at the base-emitter junction, widely used in modern devices in the place of e.g., $Al_{0.25}Ga_{0.75}As$ due to various advantages, namely, large valence band and small conduction band discontinuities, as well as lower space-charge recombination resulting from the wider bandgap, with improved performance and reliability [33–37]. The base and collector are GaAs.

In the traditional WB technology (Fig. 1b), the HBTs enjoy two metal levels referred to as M1 and M2, with M2 located over the emitter (top metal or TM style [28,29,32]). The $380 \times 300\ \mu m^2$ thinned (100-μm-thick) GaAs die is placed on an $830 \times 830\ \mu m^2$ 270-μm-thick laminate, which comprises eight $600 \times 600\ \mu m^2$ 12-μm-thick Cu plates connected by 3×3 circular Cu vias with 125 μm diameter, 200 μm pitch, and 25 μm vertical thickness, all embedded in a dielectric. The device test pads sit on the underlying substrate through a thin Si_3N_4 layer providing some thermal shunt effect [32]. Wire bonds are not present since the DUTs are designed for experimental characterization through a probing station.

Recently, high-performance technologies are moving to FC assembly, since this is assumed to offer a variety of benefits compared to the traditional WB solution, including superior thermal and electrical performance, as well as lower package height, at the price of higher cost (unless the pillar rules are kept similar to SMD); nowadays complex

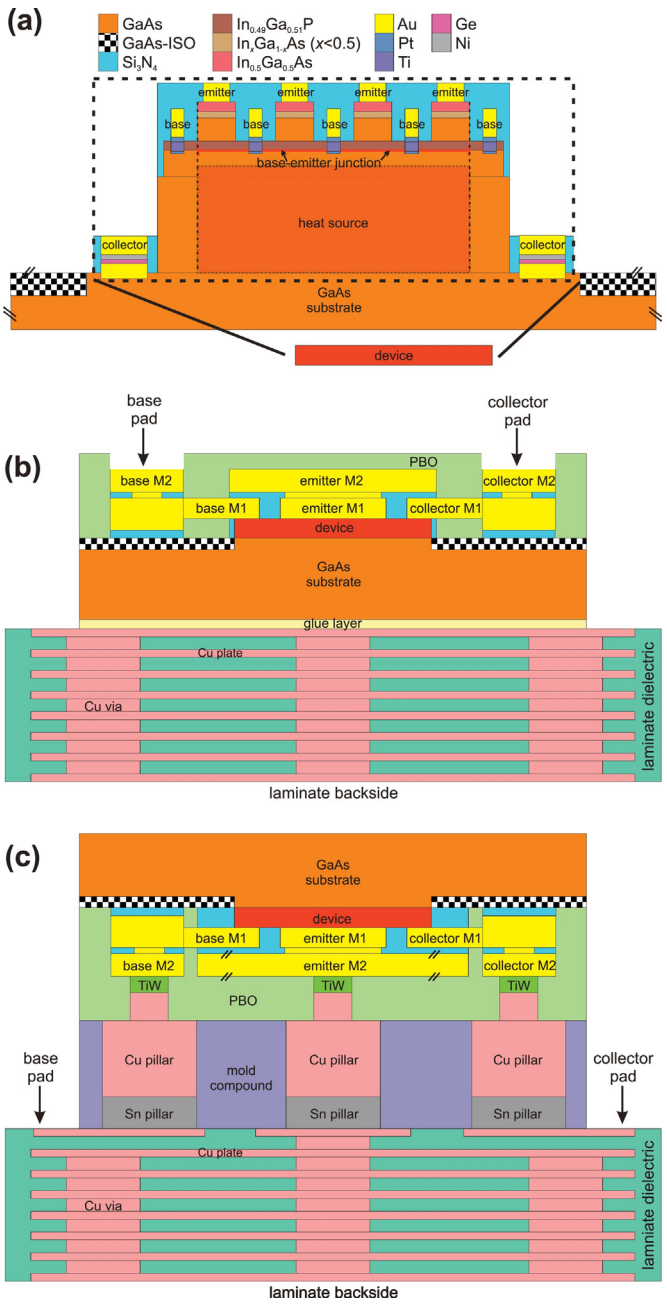

Fig. 1. Schematic cross-sections (not to scale) of (a) the intrinsic transistor region of the DUT, and of the whole DUTs (including packaging) in (b) WB and (c) FC technologies. The intrinsic region in (a) is also referred to as 'device' in (b) and (c) for the sake of clarity.

modules for several applications are fabricated using FC packaging. The FC DUT is represented in Fig. 1c; the 250-μm-thick die is flipped (i.e., the metallization faces the package), and M2 emitter, base, and collector are connected through three pillars (also referred to as bumps) to the laminate, where the pads are accessible for probing, thus allowing experimental characterization. The 80 μm-diameter pillars are composed by a 40-μm-thick Cu portion and a 10-μm-thick Sn solder, and are buried in a mold compound used as underfill material. A typical FC laminate design is adopted, which–differently from the WB counterpart–uses only a central row of three Cu vias (instead of a 3×3 arrangement), the 'inner' one being vertically located below the heat source; a lower number of thermal vias is indeed found in FC designs in order to save space for signal routing. This allows carrying out a fair comparison between WB and FC technologies.