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Estimating the Single-Event Upset sensitivity of a memory array using simulation

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ABSTRACT

This paper proposes a straightforward methodology to estimate by simulation the Single-Event Upset (SEU) sensitivity of a memory array using open source and commercial codes. It is based on a four-step process including the calculation of the deposited energy distribution in sensitive volumes, the determination of a criterion for SEU triggering, the count of SEUs, and finally the SEU cross-section calculation. The approach is validated with neutron irradiation experiments performed on a 65 nm Static Random Access Memory (SRAM).

1. Introduction

The use of memory arrays in radiation environments requires the estimation of its Single-Event Upset (SEU) sensitivity. While the most straightforward method consists in experimentally measuring this sensitivity at ground test facilities, this task can become complicated, costly or even impossible depending on the targeted radiation environment. Mixed radiation fields can require multiple tests at different facilities to account for all different radiation; some particular environments may also be unreachable in ground facilities. That is why estimating this sensitivity through simulation means is a tempting solution.

Various such simulation solutions have been proposed over the years, resulting in the development of several so-called prediction tools. [1] presents a compilation of such tools based on Monte Carlo methods, aiming at integrating all processes from the particle-matter interaction to the final response of the device. However, most of such complete tools are proprietary codes, not accessible to the general audience. Other tools use simpler methods based mostly on the Rectangular Parallelepiped (RPP) approach [2], but they thus miss the complexity of the actual shape of energy deposition. This might become an issue for today's integrated technologies [3,4]. This is why this paper mainly focuses on the SEE estimation methodology itself rather than discussing physical mechanisms of SEU triggering which are already widely documented in the literature.

In this paper, an approach is proposed to take into account all physical processes but using only open source or commercial codes. This approach is applied to Silicon-On-Insulator (SOI) technologies, and validated in comparison with neutron experimental data on a 65 nm SOI technology.

2. Description of the approach

The goal of this approach is to obtain an estimation of the Single-Event Effects (SEE) sensitivity of a memory array. This sensitivity will be represented as a SEE cross section, as a function of the incident particle Linear Energy Transfer (LET) for heavy ions, or energy for incident neutrons or protons. To calculate this cross section, four steps are needed, that are summed up in Fig. 1.

First, the studied technology is described. In particular, the sensitive areas are identified.

Second, the distribution of energy deposited in the sensitive volume is calculated for the different incident beams to consider for the study (particle, energy). This calculation is performed using a particle-matter interaction Monte Carlo simulation. A simplified geometry of the memory array is implemented and irradiated by an incident particle beam.

Third, the critical charge needed to trigger an upset is determined using an electrical simulation. A current transient is injected in the sensitive transistors of the memory point. The current characteristics are varied until the stored logic state is modified. The triggering current is then integrated to obtain a value of critical charge.

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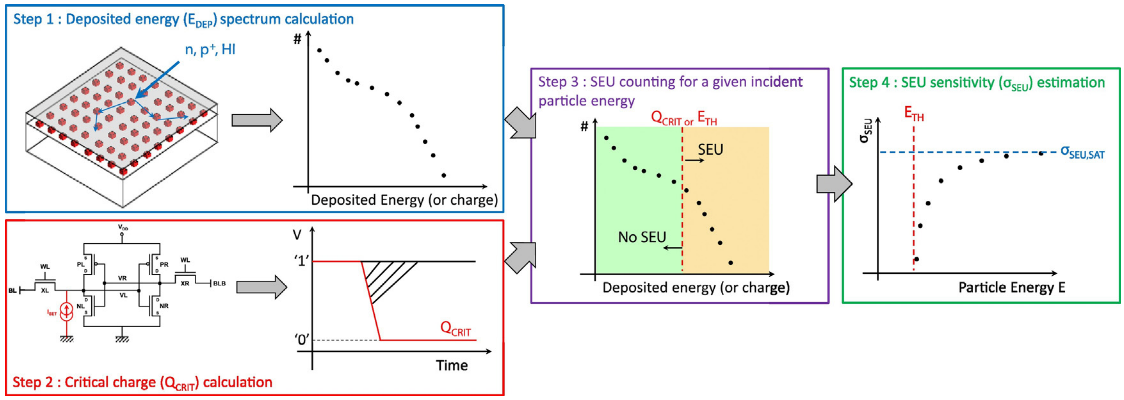

Fig. 1. Description of the SEU estimation methodology divided in four major steps: deposited energy spectrum simulation (step 1), calculation of the critical charge Q_{CRIT} to induce an SEU (step 2), SEU count using the Q_{CRIT} criterion (step 3), SEU cross-section estimation (step 4).

Finally, this critical charge, converted to an energy value, is compared to the deposited energy distribution calculated at the second step, to obtain a number of events for a given simulated fluence, particle type and energy. This is done for different distributions calculated for different incident beams, to obtain the SEU cross section vs. LET or energy curve.

These different steps are further detailed in the following.

3. Description of the device

The device is first described using the layout of a single memory point. In the following, the example of a 6T SRAM (6 Transistors Static Random Access Memory) is taken. The corresponding layout is represented in Fig. 2. In this memory point, the sensitive areas need to be identified: in a SRAM, they correspond to the two blocked transistors, identified in blue in Figs. 2 and 3.

The SRAM memory is designed in a 65 nm technology using full custom geometrical rules. In this Integrated Circuit (IC) the whole memory point geometry is voluntary relaxed in order to mitigate the onset of Multiple-Bit Upsets (MBU) due to a single particle. Both the size of the transistors and the distance between two neighbors are larger than usual ones. Except this relaxed geometry, this SRAM uses a usual 6T design. Doing this, the surface of this memory point reaches 6.15 μm^2 while the usual value for SRAM cell designed in a 65 nm technology is rather below 0.7 μm^2 [5]. The four internal transistors dedicated to the data storage (cf. PL, PR, NL and NR in Fig. 2) are located at an equal distance from the memory cell center. Only two of them are blocked to store either a '0' or a '1'. These blocked transistors define the volumes sensitive to ionizing particles. They will be used in the simulation to calculate the deposited energy and to count SEUs. The choice of a SOI technology in this study also allows having sensitive volumes perfectly defined by the surrounding dielectrics, which removes one uncertainty from the simulation results.

4. Deposited energy calculation

The deposited energy calculation is performed using the Monte Carlo particle-matter interaction toolkit Geant4 v10.1 [6–8]. One of the first steps of this calculation consists in determining the geometry to be implemented in the Monte Carlo simulation, considering both the vertical stack of different materials and the size of the sensitive volume(s). The goal of this step is to include all different materials that are likely to influence the final results, and to simplify the structure when possible.

For a SOI technology, the vertical stack will classically be simplified as the stack represented in Fig. 4(a). It includes overlayers, the active silicon film, the buried oxide and the silicon substrate. In first approximation, overlayers can be simplified in a single silica layer. A more detailed description including different layers of various materials can also be used, if such details are known for the studied technology. Even if not including such details, it is worth including high-Z material layers if their presence is known. Indeed, such materials can greatly influence the final SEU sensitivity [9], their interaction with incident protons or neutrons being susceptible to generating heavy recoil ions that will deposit particularly large values of energy in the active area. For this study, the overlayers are approximated by a silica layer, and a tungsten layer located just above the sensitive silicon film, as illustrated in Fig. 4(b).

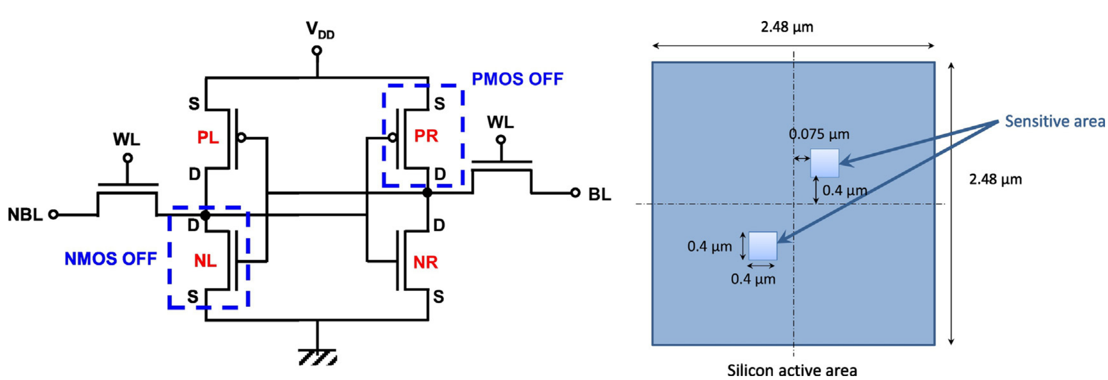

Fig. 2. Schematic description of a 6T SRAM cell. The blocked transistors (blue color) correspond to the sensitive area. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)