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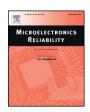
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Introductory invited paper

## Fault detection using thermal image based on soft computing methods: Comparative study

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#### ABSTRACT

This paper presents Integrated Circuit (IC) fault detection of a Printed Circuit Board (PCB) model using thermal image processing. The thermal image is captured and processed from the PCB model by the finite element method (FEM). The histogram features are extracted from the ICs hotspots which are used as inputs in a classifier model. The effective features are minimized by the principal component analysis method. In this work, a comparative study for image classification and detection is performed based on three soft computing techniques: multilayer perceptron, support vector machine, and adaptive neuron-fuzzy inference system. The effectiveness of the models is evaluated by comparing the performance and accuracy of the classification. To validate the model, the experimental evaluation is performed on Arduino UNO in order to detect the fault condition on the real time operating PCB.

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#### 1. Introduction

In recent years, the complexity of PCB implementation has increased enormously from double-sided to multi-layer PCBs. The testing and configuration times for modern PCBs continue to rise, while there is a need for production cycle times to decrease. Therefore, there is a need for new efficient methods that can reduce the amount of qualification testing in order to satisfy industrial requirements. Many of the recent techniques of configuration and testing are being processed to keep up with the increasing complexity and cost constraints of today's circuit boards and systems. One of these techniques, infrared thermal testing, is now widely used in PCB testing and fault diagnosis as a fast and effective non-destructive method of visual testing [1,2].

The infrared testing technique is very efficient in the process of manufacturing and testing of PCBs because it can monitor the thermal behavior of the IC in the PCB by sensing the emission of infrared energy (i.e. temperature) of each element. For that reason, infrared (IR) image analysis depends on the power dissipation of each IC on the PCB [3]. Some approaches have conducted temperature analysis of the PCB with different techniques of thermal imaging. Thermal analysis of a PCB is undertaken in [4]. A finite element model (FEM) via the Galerkin approach is presented to analyze the temperature behavior on the PCB for different widths of copper and different amounts of current. Also, the authors in [5] described another approach for analysis of the

thermal reliability of components on the PCB using ANSYS software to improve the reliability of the system. Thermal analysis of the PCB using MATLAB is presented in [6]. The highest temperature and maximum area of the highest temperature are used for histogram threshold analysis of the thermal image.

This work proposes a set of test techniques to decrease the test application time with different considerations. In addition, it classifies the defects of PCBs into IC level groups. Since a PCB pattern is produced in different processes, classification of defects can help in determining the sources which create errors and reduce production cost in the long run. Lastly, we arrange median with BM3D filters in series to increase the quality of IR image.

The remainder of the paper is organized as follows: the methodology of the proposed work is introduced in Section 2. Section 3 describes the PCB model developed to estimate the temperature profile of the ICs. Image processing and feature extraction are presented in Sections 4 and 5. Section 6 illustrates the classification process. Section 7 presents the simulation results. Section 8 presents the real PCB experiment results, and conclusions of this study are drawn in Section 9.

#### 2. Methodology of proposed work

The goal of this research is to develop an algorithm that is capable of testing PCBs during their manufacturing phase based on the thermal image. The present study is aimed at combining finite element modelling and intelligent fault diagnosis techniques in order to enhance IC testing for PCBs.

A simplified three-dimensional PCB finite element model is developed to estimate the temperature profile of stacked ICs. The entire

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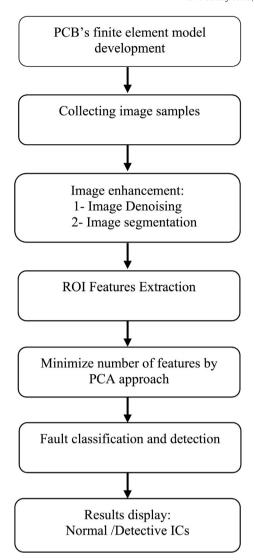


Fig. 1. Main progress steps for the proposed algorithm.

thermal simulation, applied boundary conditions, solving of the governing equations, mesh generation, and post-processing, are performed using the finite element method. Then the next step is to capture samples in different thermal conditions. Image processing with de-noising, and segmentation of the region of interest (ROI) are carried out and then the appropriate algorithm is used to extract the image features.

This work presents two sets of feature extraction from the ROI, which are first order histogram features and Gray-Level Co-occurrence Matrix (GLCM) features. Then the principal component analysis (PCA) method is applied to minimize the features extraction into the minimum uncorrelated variables, which are considered as input for the

classification program. Three common soft computing techniques; multi-layer perceptron (MLP), support vector machine (SVM), and adaptive neuron-fuzzy inference system (ANFIS), are used to classify the fault conditions of ICs into two classes as normal or faulty. We adapt the capabilities of MATLAB to achieve the above steps. Fig. 1 shows a flowchart containing the methodology undertaken in this work.

#### 3. The PCB module

In this section, the process of finite element modelling (FEM), including 3D PCB geometry, the physical properties, and study of the thermal profile are presented. The thermal profile for the proposed PCB is extracted from the thermal characteristics of the Atmel standard [7]. The simulation process comprises the following essential steps.

#### 3.1. Physical model generation

The geometric model of the PCB with three main chips is created. Table 1 lists the main geometric dimensions of the PCB. The first chip is the simplified Plastic Dual Inline Parallel (PDIP). This type is a rectangular-shaped package with two parallel rows of electrical connecting pins coming out of the two sides of the package. The basic geometric shape is imported from the COMSOL library [8].

The computational time can be reduced by ignoring the details of copper wires, and other electronic elements in the PCB. This can be carried out because the equivalent FE model is related to simulating the temperature distribution on the ICs surface.

The other chip packages, chip 2 and chip 3, act a simplified geometry for a Plastic Quad Flat No lead (PQFN) [7,8]. This type of package is a surface-mounted device and must be mounted directly on the surface of the PCB, and connections from the pins to the tracks of the PCB are made on the same side as the package is mounted. In this study, it is assumed that there are no differences in the heat conduction of the leads and pins of the chips. The geometry model of the PCB is shown in Fig. 2.

#### 3.2. Physical materials and thermal properties

The next analysis process of the FEM is defining the layer types and material properties in the PCB modelling. Initially, the 3D PCB model consists of five main parts, as follows:

- First part: FR4 material (i.e. fiberglass in an epoxy resin) from which the PCB board is made.
- Second part: die element acts as the silicon IC layer.
- Third part: bond wires and lead frame layer, with the material (i.e. copper material layer).
- Fourth part: mold (i.e. package) covering the contact material and die elements.
- Fifth part: air is the empty space between PCB surface and IC1 of the PCB

Generally, thermal conduction and convection affect the heat diffusion of the ICs on the PCB board. The electric power drawn by the PCB

**Table 1** PCB geometry dimensions.

Component		Dimensions ( $\Delta x \times \Delta y \times \Delta z$ ) mm <sup>3</sup>			
			IC1	IC2	IC3
Layout 1	PCB	$70 \times 55 \times 4$	_	=	-
Layout 2	Die	_	$2 \times 2 \times 0.1$	$2 \times 2 \times 0.3$	$1 \times 1 \times 0.15$
Layout 3	Mold package	_	$10 \times 3.427 \times 1$	$6 \times 6 \times 1$	$2.4 \times 2.4 \times 1$
Layout 4	Bond wires and lead frame	-	$(2.358 + 1.949 \times 16)^{a}$	$3\times3\times0.2$	$1.5\times1.5\times0.1$

<sup>&</sup>lt;sup>a</sup> Bond wire + lead frame  $\times$  no. of pins.

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