Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory invited paper

Improved on-chip self-triggered single-event transient measurement circuit design and applications

Rongmei Chen [a,*], Wei Chen [b], Xiaoqiang Guo [b], Chen Shen [c], Fengqi Zhang [b], Lisang Zheng [c], Wen Zhao [b], Lili Ding [b], Yinhong Luo [b], Hongxia Guo [b], Yuanming Wang [b], Yinong Liu [a]

[a] Key Laboratory of Particle & Radiation Imaging, Ministry of Education, Department of Engineering Physics, Tsinghua University, Haidian District, Beijing 100084, China
[b] State Key Laboratory of Intense Pulsed Irradiation Simulation and Effect, Northwest Institute of Nuclear Technology, P.O. Box 69-10, Xi'an 710024, China
[c] Cogenda Co Ltd., SISPARK II Room C102-1, 1355 Jinjihu Avenue, Suzhou, Jiangsu, China

ARTICLE INFO

Article history:
Received 1 December 2016
Received in revised form 6 March 2017
Accepted 6 March 2017
Available online xxxx

Keywords:
Single-event transient (SET)
Combinational logic
SET pulse width
Pulsed laser

ABSTRACT

Single-event transient (SET) induced soft errors are becoming more and more a threat to the reliability of electronic systems in space. The SET pulse width is an important parameter characterizing the possibility of an SET being latched by a sequential element such as a flip-flop. This paper improves the widely used on-chip self-triggered SET measurement circuit by changing it from a single SET measurement module to a combination of two modules. One module is responsible for measuring narrow SET pulse widths while the other is responsible for measuring modest and wide SET pulse widths. In this way, the range of measurable SET pulse width is increased. Pulsed laser facility is used to simulate single-event transients induced by single-particles. Experimental results demonstrate that the minimum accurately measured SET pulse width is decreased from 166.5 ps to 33.3 ps after adopting the proposed design when compared with the original one. SET pulse width broadening effect was also observed using the measurement system. The broadening factor was measured to be 0.123–0.143 ps/inverter.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

Single-event effects (SEEs) are becoming more significant as the technology node of semiconductor integrated circuits (ICs) improves for several reasons. First of all, the decrease of parasitic capacitance of a sensitive node in an integrated circuit leads to the reduction of SEE critical charge, increasing the SEE sensitivity to the strike of a high energy particle into the node. Secondly, the density of IC increases a lot with technology improvement, reducing the distance between two sensitive transistors. It leads to charge sharing effect and makes single-event upset (SEU) spatial hardening technique like DICE [1] become ineffective gradually. [2] found that the decrease of proton and neutron flip-flop SEU cross section after adopting DICE structure is only about 60% in comparison with conventional flip-flop. Thirdly, the sensitivity of logic circuit to single-event transient (SET) is significantly increased. N. N. Mahatme et al. [3] found that soft errors resulting from SETs in combinational logic circuit have surpassed those from SEUs in flip-flops and memories like SRAMs when the combinational logic circuit operates at high frequency. There are several reasons that explain the increased contribution of SET induced soft errors. What is more, SET induced soft errors can't be mitigated by the Error Check and Correction (ECC) technique [4]. ECC is only effective for the memory components in an IC.

As the technology improves, the working frequency of ICs increases a lot. The probability of an SET to be latched by a sequential element like flip-flop is proportional to the SET pulse width and frequency simultaneously [5]. As a result, an SET of the same width is easier or of higher probability to be latched by a flip-flop and produces a soft error when frequency increases. Meanwhile, the speed of ICs also improves with technology. The electrical masking effect is thus less prominent and SET of narrower pulse width is able to propagate in combinational logic without attenuation as [6,7] discussed.

As noted above, the SET pulse width is an important parameter that characterizes the possibility of an SET to be transferred to a soft error. Many techniques have been proposed to measure SET pulse width. All techniques can be classified into two classes: on-chip and off-chip. Off-chip method makes use of an external instrument such as a high-speed oscilloscope [8]. This technique has the ability of observing and catching the detailed shape of an SET but it is difficult to detect very narrow SET pulse due to the limit of a high-speed oscilloscope and to the signal distortion from the chip to the oscilloscope. On-chip technique, however, makes the combinational logic (source of SETs) and the measurement circuit integrated in the same chip, thus avoiding the problem of signal disruption when the signal is propagated out of the chip.

* Corresponding author.
E-mail address: mei2008011733@126.com (R. Chen).

http://dx.doi.org/10.1016/j.microrel.2017.03.004
0026-2714/© 2017 Elsevier Ltd. All rights reserved.

Please cite this article as: R. Chen, et al., Improved on-chip self-triggered single-event transient measurement circuit design and applications, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.03.004

ARTICLE IN PRESS

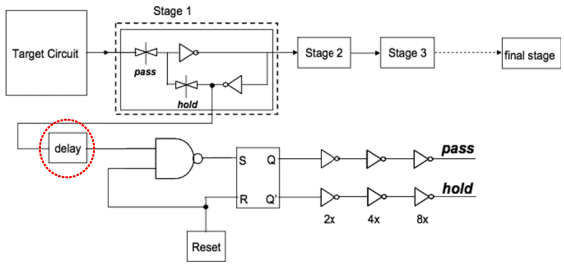

Fig. 1. On-chip self-triggered SET measurement circuit schematic [16].

The on-chip SET measurement design developed by [9] has been widely used by researchers [10] and [11] for its simplicity and high resolution. However, it is not able to accurately detect SETs which are so narrow that they attenuate along the SET measurement circuit. The minimum pulse width for unattenuated propagation through an infinite number of logic gates is about four times the propagation delay of a single logic gate [12]. Narrow SET pulse width that can't propagate without attenuation may account significantly for heavy ion irradiation with particle LET (linear energy transfer) of more than 49 MeV·cm^2/mg as presented by Loveless et al. [13]. In order to overcome this shortage, this paper develops and designs an improved SET pulse width measurement design based on the original one. It not only solves the problem of narrow pulse width measurement but also simplifies the design of self-triggered part of the SET measurement circuit.

2. SET propagation simulation

Different from SEU, SET produced in the combinational logic circuits is not directly interpreted as a soft error. It needs to propagate along the following combinational logic after its production and meet a flip-flop before being latched and producing a soft error. So, the propagation principle of SET plays an important in determining the possibility of SET-induced soft errors. V. Ferlet-Cavrois [8] found that floating body effect in partial depleted silicon on insulator (PD SOI) process leads to broadening of SET pulse width along combinational logic [14]. It is because of the threshold voltage hysteresis effect under the static or semi-static SET measurement condition [15]. In bulk process, the effect is not obvious. However, by contrast, SET pulse width is reduced gradually if the width is narrower than a threshold value in whatever technology. As Massengill studied in [15], the threshold pulse width is the sum of output rise time and fall time of a combinational logic unit when input with a square pulse. On-chip self-triggered SET measurement circuit [9,16] is

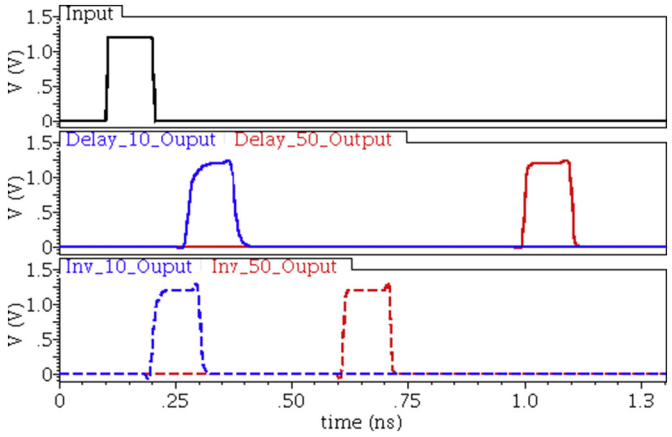

Fig. 2. SET of 100 ps pulse width propagates along two different combinational logic chains: the injected SET and the SETs after propagating to 10th and 50th stages in the two chains.

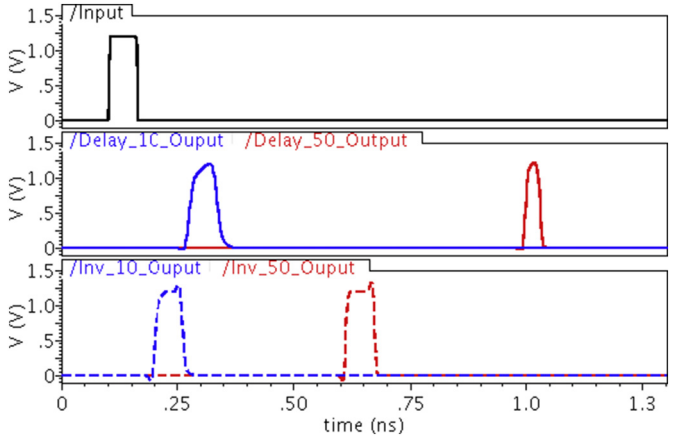

Fig. 3. SET of 60 ps pulse width propagates along two different combinational logic chains: the injected SET and the SETs after propagating to 10th and 50th stages in the two chains.

based on the propagation of an SET along a transparent latch chain and a capture of latches' states when the SET in still on the chain, as shown in Fig. 1. By counting the number N of transparent latches being influenced by an SET and obtaining each latch delay τ, the SET pulse width can be determined to be $N * \tau$. In order to make sure that an SET propagates to the end part of the transparent chain before propagating out of it, delay (as highlighted in the red circle) in the self-triggered circuit should be carefully designed.

Logically speaking, a transparent latch is an inverter but is essentially of larger electrical response time, including the rise time and fall time as mentioned earlier. This is because each transparent latch consists of two inverters and two pass gates with large parasitic capacitance in the signal propagation path as detailed in the dotted rectangle in Fig. 1. As a result, a narrow SET propagated along a transparent latch chain is easier to be attenuated than that along an inverter chain of similar sizes. Fig. 2 shows that an SET of 100 ps pulse width propagates along a transparent latch chain and along an inverter chain. Both chains are designed with similar transistor sizes. Since its pulse width is large enough, the SET propagates along both chains without attenuation. Nevertheless, an SET of 60 ps is attenuated along the transparent latch chain while not attenuation is observed in the inverter chain, as shown in Fig. 3. Further simulation shows that the threshold pulse widths of which an SET is able to propagate without attenuation for the transparent latch chain and the inverter chain are 80 ps and 45 ps respectively. Because of the significant difference of threshold SET pulse widths for an inverter chain and a transparent latch chain, some narrow SETs (in the range of 80 ps–45 ps) which are produced and propagate without attenuation in combinational logic are attenuated in the SET measurement circuit and thus can't be measured accurately.

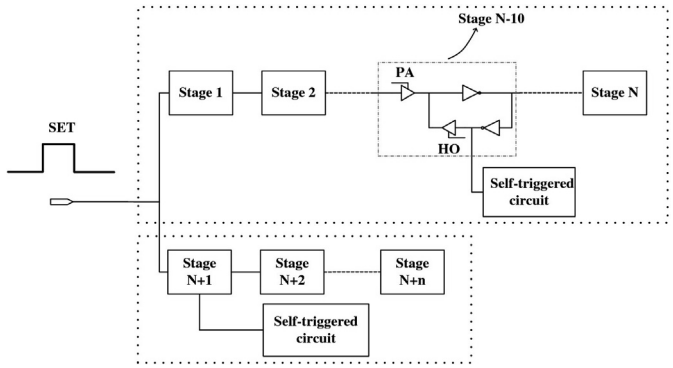

Fig. 4. Schematic of the proposed on-chip self-triggered SET measurement circuit.

Please cite this article as: R. Chen, et al., Improved on-chip self-triggered single-event transient measurement circuit design and applications, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.03.004

Download English Version:

https://daneshyari.com/en/article/4971469

Download Persian Version:

https://daneshyari.com/article/4971469

Daneshyari.com