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# Single event transient effects on charge redistribution SAR ADCs ☆

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ABSTRACT

This work presents a study on the effects of Single Event Transients on Successive Approximation Register Analog-To-Digital Converters (ADC) based on charge redistribution. The effects of SETs are analyzed by means of an extensive fault injection campaign by using a SPICE simulator and a predictive 130nm CMOS technology model. Faults are injected in the analog blocks and in the digital control circuit of the converter. Results show that the transient effects may change the state of one or more bits of conversion, since the affected conversion stage may propagate an incorrect value to the remainder of the conversion, leading to multiple bit errors on the converted data. Results also allow to identify the most sensitive nodes and the failure mechanisms associated to transient effects on this type of converter. Finally, some design-level mitigation strategies are applied, in a way that the error rate and the magnitude of conversion errors are significantly reduced.



## 1. Introduction

The choice of an appropriate data converter by the designer of mixed-signal systems is usually made considering factors like power consumption, total silicon area, resolution and conversion speed. Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) comprise one of the most popular topologies used in integrated circuits because it presents a good compromise among these features. Though not suitable for designs requiring a very high resolution, it has low power consumption, low area, and good conversion speed [1]. One of the possible implementations of SAR ADCs consists in the concept of charge redistribution, which provides several advantages compared to the conventional SAR topology, such as the reduction of passive devices mismatch on the CMOS process due to the introduction of a capacitive array.

SAR ADCs are sequential converters that take N clock cycles to convert an analog input into an N-bit digital representation. They are frequently chosen over flash ADCs for medium to high-resolution applications, since flash ADCs over 10 bits are not commercially viable [2]. Additionally, SAR ADCs usually present better conversion speed than Sigma-Delta converters [1], though reaching lower resolutions. SAR converters are present on several commercially available programmable mixed-signal platforms, such as PSoC5 [3], SmartFusion [4] and MSP430F6638 [5].

The low power feature of this kind of converter may be a desired benefit for critical applications such as satellite control and instrumentation systems, and wireless sensor networks, for example. These applications may be subjected to environmental interactions, such as radiation effects and electromagnetic interference, and, despite that, it is desirable that these embedded converters perform correctly in such conditions.

One example of such harsh operation conditions are applications susceptible to ionizing radiation. When an ionizing particle collides with one or more transistors of the converter, a transient effect may occur. These effects, known as Single Event Transients (SETs) are caused by the collection of charges on reverse biased P–N junctions of the semiconductor after a heavy ion strike or indirect ionization [6]. At electrical level, these effects generate voltage or current pulses that may propagate into combinational or analog circuits or even be captured by registers or directly invert the state of storage elements, generating single event upsets (SEUs).

The basic building block of charge redistribution SAR converters is a capacitor array controlled by a set of switches. The effects of transient faults on programmable capacitor arrays (PCAs) were first addressed in Ref. [7]. In that work, it is demonstrated that SETs in the switches of the PCA may lead to an unintended charge redistribution process, modifying the voltage stored in the capacitors. Experimental results of neutron irradiation test on a commercial programmable SoC containing an SAR ADC based on charge redistribution are addressed in Ref. [8].

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Indeed, in the past years several commercial available charge redistribution SAR ADCs were tested under single event effects with neutrons and heavy ions. Most of available papers present only cross section and latchup data, as, for example, Refs. [9–11]. However, some of them present also data regarding the behavior of the converter output [12–16] which are in accordance with the simulation results of this paper as will be detailed in the results of this paper (Section 5).

This is the first work where a deeper investigation of the transient effects on SAR ADCs is presented, addressing architectural and algorithmic aspects. The proposed analysis consists in a fault injection campaign on the sensitive nodes of the converter, both in its analog and digital parts. Results allow to identify the most sensitive nodes of the circuit to transient effects and error mechanisms. Radiation-hardening techniques are then proposed.

Fault injection was performed by means of SPICE simulations, modeling the SETs as current sources connected to the drain of the transistors, according to the model developed by Messenger [17] and the simplified fault injection scheme described in Ref. [6]. The results of the conversions are analyzed for a worst-case width and amplitude of the current pulse, considering a predictive technology model (PTM) of the 130 nm node [18].

## 2. Charge redistribution SAR ADCs

The classical circuit of charge redistribution ADCs was proposed by McCreary and Gray [19] in 1975 and became one of the most popular architectures for ADCs that require low silicon area and low power consumption. These features are achieved because the capacitor array replaces the Digital-To-Analog (DAC) converter required to generate the reference voltage levels on traditional SAR converters. This circuit is outlined below:

### 2.1. Main architecture

The circuit of the charge redistribution SAR ADC consists of four main blocks: a capacitor array, a comparator, a set of switches, and the digital control logic for the switches.

The capacitor array consists of N + 1 binary-weighted capacitors, where N is the number of bits of the converter. Each bit is associated to one capacitor, and due to the binary-weighted scheme, increasing the resolution will cause a penalty on the area of the circuit, since each additional bit increases the overall capacitance by a factor of two. This approach may limit the implementation of this topology for high-resolution converters.

The simplified schematic of the converter is shown in Fig. 1. The design of the capacitors requires a total capacitance of 2C, where each capacitor is multiple of $C_{Unit}$ and the capacitance is given by the following:

$$C_N = 2^N \times C_{Unit} \tag{1}$$

where $C_N$ is the capacitance associated with the $N$th bit. An additional unit capacitor is added to allow the total capacitance to be even with respect to $C_{Unit}$ ($C_{0'}$ in Fig. 1; where $C_{0'} = C_0 = C_{Unit}$). This way, binary weighted capacitive dividers are achieved during the charge redistribution phase.

### 2.2. Mechanism of conversion

The conversion is performed by a sequence of comparisons of the input signal with quantization levels generated by the reference voltage through the capacitive dividers formed by the switching scheme, converging to an equivalent digital representation.

A comparison of the signal to these values are performed on a comparator, which will output "HIGH" if the input voltage is higher than the weighted reference voltage, or "LOW" otherwise. The output of the comparator will control the weighting of the reference voltage to allow the convergence of the digital output. The control logic then implements the algorithm that performs the correct switching scheme for the circuit.

The algorithm of conversion for a charge redistribution SAR converter is outlined below:

1) *Sample and hold*. The operation of the circuit starts when the parallel association of all capacitors is charged to a value equivalent to the input voltage. This requires that all switches connected to the bottom plates of the capacitors must be switched to the common bus, which, in this phase, is connected to $V_{IN}$, while the top plates are connected to $V_{REF}$. When the sampling signal (i.e. the signal that resets the control logic) is enabled, the switch common to the top plates of the capacitors is open and the switches of the bottom plate of each capacitor are connected to ground.
   Therefore, the voltage at the top plates of the capacitors (connected to the negative input of the comparator) after the sample and hold phase is expressed as follows:

$$V_{comp-} = V_{REF} - V_{IN} \tag{2}$$

   leading to the storage of an equivalent charge, proportional to the absolute value of the analog sample ($V_{IN}$), as follows:

$$Q = 2C \times (V_{REF} - V_{IN}) \tag{3}$$

   where 2C is the total capacitance of the array. In this work the total capacitance of the array of the studied converter is 2C= 3.072 pF, with an unit capacitance of 12 fF.The reason to sample the input signal related to $V_{REF}$, instead of ground, is to avoid a negative voltage between the $V_{comp-}$ node and ground. This is due to the fact that, when MOSFET switches are used, a negative voltage at this node might turn back on the NMOS transistor (which connects the capacitors to ground) during the hold phase, discharging the array (the design studied in this work employs NMOS switches and transmission gates as detailed in Fig. 6, Section 4). The voltage $V_{REF}$ is then canceled out at the output of the comparator by comparing the held voltage to $V_{REF}$. In this work $V_{REF} = V_{DD} =$ 1.2 V.
2) *Charge redistribution*. The conversion starts by turning the $V_{IN}/V_{REF}$ switch to $V_{REF}$ and the switch associated with the most significant bit (MSB) – in this case, switch $S_7$ – to the common bus. This generates a capacitive divider between the capacitor $C_7$ and the parallel association of $C_6 - C_{0'}$. Due to the binary-weighted nature of the array, a capacitive divider between two equal capacitances is obtained. Considering the specific capacitance values of the design adopted in this study, both capacitors have an equivalent value of $C = 1.536$ pF. This allows an equivalent voltage of $V_{REF}/2$ to be added to the voltage on the common node.

A comparison is then performed between $V_{REF}$ and $(V_{REF} - V_{IN}) + V_{REF}/2$. If $V_{IN} > V_{REF}/2$, the comparator will output a logical "HIGH" level, which indicates that the MSB is "1". This output controls the switching scheme for the next step of conversion. A logical "HIGH" level on the output allows the control logic to connect switch $S_6$ to bus, keeping $S_7$ also connected to the bus. This operation indicates that, if the analog input is higher than the midscale (higher than $V_{REF}/2$), the next stage will determine whether the signal is lower or greater than 0.75 $V_{REF}$. On the other hand, a logical "LOW" level