Microelectronics Reliability 73 (2017) 60–68

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Monitoring of thermo-mechanical stress via CMOS sensor array: Effects of warpage and tilt in flip chip thermo-compression bonding

Ari Laor [a], Depayne Athia [a,*], Alireza Rezvani [b], Horst Clauberg [b], Michael Mayer [a]

[a] Microjoining Laboratory, Centre for Advanced Materials Joining, Department of Mechanical and Mechatronics Engineering, University of Waterloo, Waterloo N2L 3G1, Ontario, Canada
[b] Kulicke & Soffa Industries Inc. Fort Washington, 19034, PA, USA

ARTICLE INFO

Article history:
Received 11 January 2017
Received in revised form 2 March 2017
Accepted 3 March 2017
Available online xxxx

Keywords:
Thermo-compression bonding
Flip Chip
Piezoresistive
Advanced packaging
Warpage
Tilt
Au bumps
Reliability
Interconnect
Thermal gradient

ABSTRACT

Flip chip thermo-compression bonding (TCB) involves the use of heat and pressure to simultaneously form interconnections for microelectronic packaging. In-situ measurements of thermo-mechanical stresses that arise during this bonding process could provide unique insight to help better understand the TCB process. A 4 mm × 3 mm × 500 μm complementary metal-oxide-semiconductor (CMOS) sensor chip with an 8 × 8 array of Au-bumped sensor pads was developed for this purpose. It was designed to record XYZ force and temperature signals from bump locations, during a simulated flip chip process similar to TCB.

In-situ measurements during simulated TCB events proved useful for tilt detection, thermal gradient characterization, and thermal expansion measurements. Further interpretation of the signals proved tilt and other thermo-mechanical effects were induced by thermal expansion mismatches. The most thermo-mechanically stressful stage of bonding was found to occur during thermal transients, specifically during bond head ramping. Further analysis concluded the actual time necessary to heat the bumps was less than 0.5 s. Finally, the lateral thermal gradient across the sensor chip was calculated to be smallest in the central bump locations, and largest in the bump array corners due to warpage, tilt, and heat sink effects of the digital logic region.

1. Introduction

To further miniaturize microelectronics, interconnect technologies have been shifting towards advanced TCB methodologies [1–6]. TCB is similar to classical flip chip bonding, but uses copper pillars instead of solder balls. The most common chip sizes range from 10 mm × 10 mm with several hundred [1] or thousand [2–5] bumps to smaller chips with less than ten bumps for MEMS applications [6].

The advantage of TCB interconnects is the simultaneous and area-array nature of the bonding process allowing for larger number of I/Os and finer pitches compared to wire bonding. However, there are also challenges during the TCB process due to the combination of typical process parameters: force, heat, and time [7–8]. The challenges include thermal coefficient of expansion mismatches, temperature gradients, misalignment, tilt and other process factors introducing stress and warpage [3–6]. Global warpage and stress introduced by thermal coefficient mismatch and/or bond head force/heat gradients lead to more complicated process window determination [2,4,5].

Tools for measuring temperature and stress in-situ during wire bonding were demonstrated in [9–16]. These tools were developed and were comprised of piezoresistive and RTD elements to integrate force and temperature sensors via CMOS processes. Development of these sensors led to an enhanced understanding of CMOS processes and further optimization of sensor design to produce better suitable tools for measurement purposes. While TCB typically uses copper pillars, Au bumps were used for our purposes to simplify earlier stages of experimental procedures with this newly developed sensor chip. This approach laid essential groundwork derived from mastering the operation of the sensor chip. It also helped to identify any downfalls or issues to be addressed. Both of these considerations could be used for continued research. This work reports on the development of this new sensor tool to perform in-situ measurements during simulated TCB events to learn more about the process challenges and ways to overcome them.

2. Experimental setup

2.1. Design of CMOS sensor chip

A ⟨100⟩ Si wafer, four metal mixed signal 0.35 μm CMOS process from AMS was selected to design the layout of a sensor chip approximately 4 mm × 3 mm in size, as shown in Fig. 1. Standard library, 95 μm square Al CMOS bond pads were arranged into a 400 μm pitch 8 × 8 array. There are serial data buses available at each pad to distribute the differential force signals and RTD signals. The switches were realized using

* Corresponding author at: University of Waterloo, 200 University Avenue West, N2L 3G1, Waterloo, ON, Canada
E-mail address: dathia@uwaterloo.ca (D. Athia).

http://dx.doi.org/10.1016/j.microrel.2017.03.001
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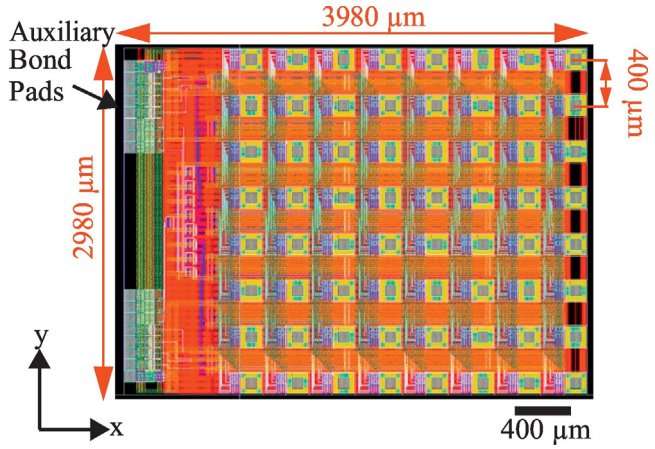

Fig. 1. CMOS Sensor Layout with a total of 64 Sensor pads, all pads with local RTD in top metal. 30 of the pads have Z stress sensors, 17 have X sensors and 17 have Y sensors available.

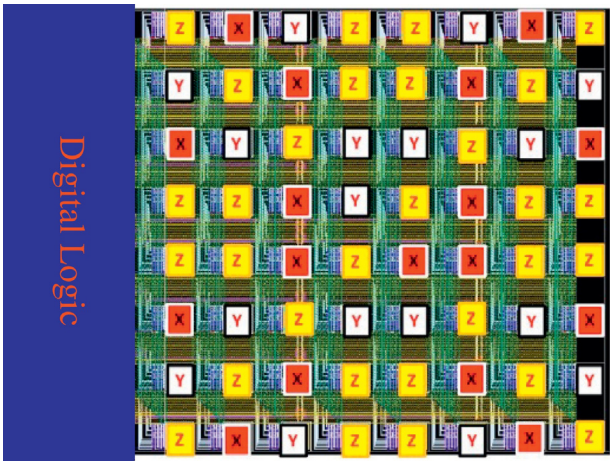

Fig. 3. Locations of XYZ Sensors on CMOS sensor chip.

transmission gates and their respective "on" resistance is 1024 Ω. A single pad can be switched onto the bus with the on-chip multiplexer by programming the corresponding address. Consequently, only one pad is switched at a time with a 1 ms resolution between pad to pad switching. Therefore, the cycling of all 64 pads takes 64 ms. Each of these bond pads is surrounded by a local RTD sensor (Fig. 2a, b, c) consisting of a serpentine structure of top metal Al to be used in conjunction with similar fourwire or Kelvin measurement techniques as discussed in [9–12] with lead resistance elements that include CMOS switching. The RTD gives the average temperature in the area covered by the serpentine lines around the bond pad. In addition, the pads have one of either an X, Y, or Z force sensor element made of piezoresistive n+ or p+ diffusions as shown in Fig. 2d and e. The locations of the X, Y, and Z sensors on the layout of the chip are illustrated in Fig. 3. The sensors are based on the designs introduced in [12] and [14]. Such an arrangement detects stress originating from the center of the bond pads and sensitizes them to exclusively one of the X, Y, or Z forces. Resistor elements *Ra* and *Rd* are located oppositely to *Rb* and *Rc* in a Wheatstone bridge configuration as shown in Fig. 2f. This configuration also allows the sensor to reject common noise seen at the resistor elements.

2.2. Packaging of TCB sensor array

In order to read an in-situ signal from the CMOS chip during a simulated TCB event, auxiliary bond pads were placed 1 mm away from the 8 × 8 sensor arrangement as illustrated in Fig. 4. An automatic ball-wedge bonder was first used to create standard 25 µm 99.99% pure Au wire bonds, establishing chip-to-substrate connectivity while also delivering power to the CMOS circuit. The unpackaged sensor chip is shown in Fig. 5a, after die attach, in Fig. 5c and after wire bonding in Fig. 5d. The same Au wire was also used to deposit 68 µm diameter

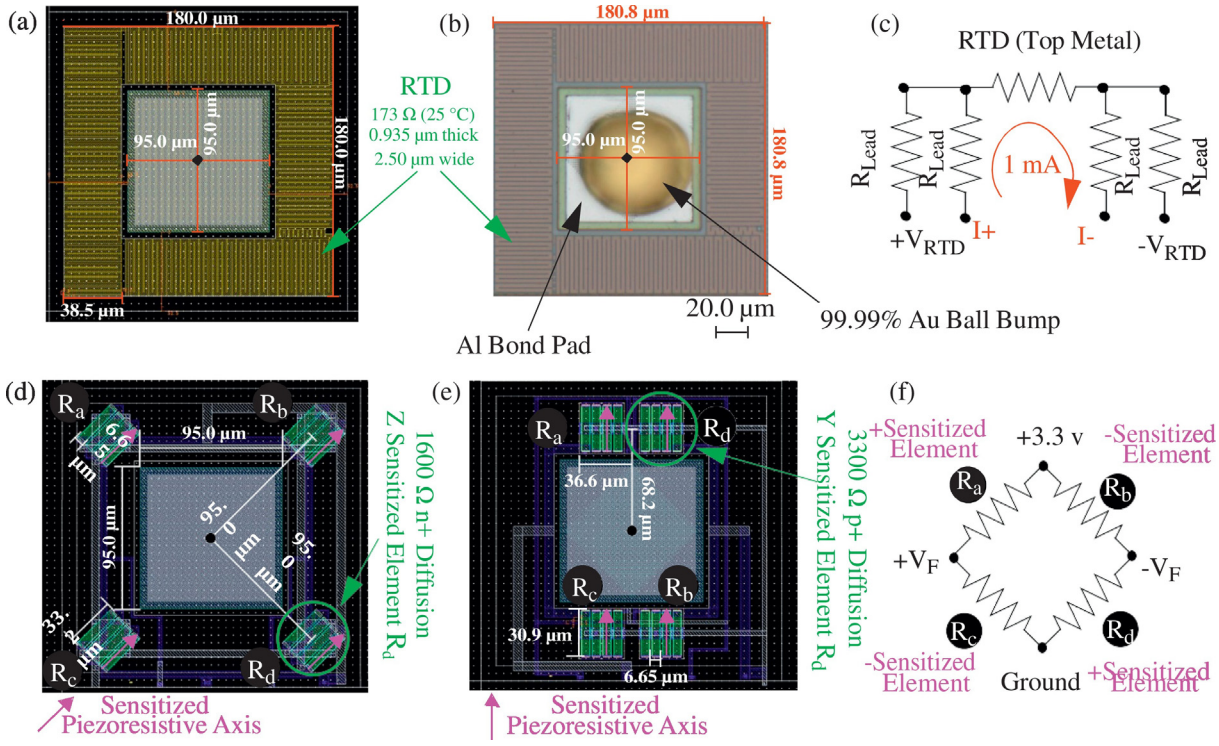

Fig. 2. (a) RTD sensor layout around the 95 µm square pad. (b) Micrograph of RTD sensors with Au bump on pad. (c) Schematic view of RTD sensor. (d) Z sensor layout. (e) Y sensor layout (X is identical, but rotated 90°). (f) Schematic view of force sensor Wheatstone bridge.