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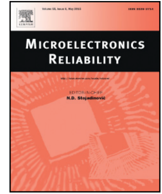

Static fault localization of subtle metallization defects using near infrared photon emission microscopy

A.C.T. Quah *, D. Nagalingam, S. Moon, E. Susanto, G.B. Ang, S.P. Neo, J.C. Lam, Z.H. Mai

Product, Test & Failure Analysis, GLOBALFOUNDRIES Singapore Pte Ltd., Singapore

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A B S T R A C T

In this paper, two electroluminescence phenomena, which enabled the static electrical fault localization of subtle back-end-of-line metallization defects using near-infrared photon emission microscopy in the logic circuitry and the memory array, are described. In the logic circuitry, through the study of the defect-induced hot carrier emissions from the combinational logic gates, distinctive differences in emission characteristic between open and short defects are identified. Using this defect induced emission characterization approach, together with layout trace and analysis, the type of defect can be predicted. The defect physical location, which yielded no detectable hotspot signal, can also be narrowed down along the long failure net. This allows for the selection of the most appropriate physical failure analysis approach for defect viewing and thus achieving significant reduction in failure analysis cycle time. In the memory array, the weak emission from partially turned-on pass gate transistor is leveraged to localize marginal opens and shorts on the wordline node of the pass-gate transistor. These approaches are applied with great success in the foundry environment to localize yield limiting defects that resulted in SCAN and memory build-in self-test failure, without memory bitmap, diagnostic support or measurable I_{DD} leakage, on advanced technology nodes devices. A discussion on the factors that influence the success rate of this approach is also provided.

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1. Introduction

Failure analysis (FA) is an integral step for the development and manufacturing of semiconductor integrated circuits (IC) and fault localization is the most crucial step in the entire FA cycle. In the wafer foundry industry, a marginal process drift could result in severe yield loss and excursion which leads to wafer scrap and loss in revenue. Thus, early inline detection and short FA cycle time are critical to maintain line quality and profitability.

The continuous scaling of semiconductor integrated circuits (IC) technology as according to ITRS roadmap [1], drives the reduction in the critical defect size. Consequently, in today's advanced ultra-large-scale IC devices, a marginal process drift resulting in yield loss would surface evidently in functional logic and memory failure modes, like SCAN and memory built-in self-test (BIST), where the minute defect falls among the dense signal nets and memory cells, rather than impacting the power supply rails causing V_{DD} to V_{SS} shorts or leakages. Thus, conventional static fault localization approach that is limited to the biasing of a few power supplies and ground pins and the use of laser induced power alteration techniques like Thermal Induced Voltage Alterations (TIVA), Optical Beam Induced Resistance Change (OBIRCH) [2] to localize metallization resistive defects are no longer effective enough for yield debug. This is worsen with the increasing ease of causing laser induced damage which limits the laser power [3] and reduces on the techniques' detection sensitivities. While near-infrared photon emission microscopy (NIR-PEM) is also an established static fault localization technique, it is more effective for isolating front-end-of-line (FEOL) defects relating to junction leakages, anomalous junction formation and gate oxide breakdown [4,5]. It is however, ineffective in localizing ohmic shorts and opens in the back-end-of-line (BEOL) metallization stack as these defects either do not emit photons or the thermal emissions are too weak to be detectable by the InGaAs photon detectors with sharp detection wavelength cut off at ~1.5 μm, unless there is sufficient Joule heating effects from a defect drawing sufficiently high current density [6].

The *de facto* methods for debugging memory BIST and SCAN failures relied heavily on memory bitmapping and commercial scan diagnosis tools [7] like TetraMAX and Tessent, respectively. These are categorized as software-based fault isolation methods. For memory bitmap, the memory scrambling and design information are needed, usually from external embedded memory intellectual-property (IP) providers, to obtain the failure bits addresses. While for software scan diagnosis, scan log, pattern file and design information are needed for the software compiler to deduce the logic failure net and cell for subsequent physical

* Corresponding author.
E-mail address: Alfred.QUAH@globalfoundries.com (A.C.T. Quah).

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failure analysis (PFA). Both approaches required additional cost and resources to be enabled.

In the event that software-based fault isolation methods are not available or insufficient, a large variety of dynamic electrical fault isolation techniques and its variant have also been developed using the hardware-based approach to localize both hard and soft defects. These techniques include dynamic photon emission [8], Electro Optical Frequency Mapping (EOFM) [9–11], Thermal Frequency Mapping [12,13], laser voltage probing (LVP) [14], soft defect localization (SDL) [15], Light Assisted Device Alteration (LADA) and its derivatives [16,17]. These techniques are implemented in a heavy instrumentation environment where expensive analytical scanning optical microscope system is docked with commercial tester and the test program is used to exercise the device to its specific functional failure state on hold or on continuous looping for fault localization. This is followed by further circuit and layout analysis to interpret and correlate the signal with suspected failure mechanism before arriving on suspected defective net or location for subsequent PFA. Due to the complexity in test setup, device characterization, signal capturing (typically with the application of solid immersion lens for enhanced spatial resolution) and signal interpretation, dynamic fault localization approach is more time consuming than the static fault localization approach where only 2–3 probes are needed.

For these dynamic electrical fault isolation techniques to be enabled in the wafer foundry environment, besides large instrumentation investment, device test program, test patterns, production probe card, device test board and certain design specific information have to be shared by the customer. Thus, although these techniques are effective and critical in assisting the wafer foundry to accelerate low yield investigation, excursion debugging and new product manufacturing yield ramping, they may not be available to support every product due to cost avoidance or IP confidentiality reasons. This has posed great challenges for foundry in fault localization, especially on subtle defects resulting in functional logic failure like SCAN and memory BIST in advanced technology nodes with marginal or no leakage signature observable in the power domains.

In this paper, the effectiveness of static fault localization on functional logic and memory failures, without observable I_{DD} leakages, are significantly enhanced with the detection of weak electroluminescence from the sensitized combinational logic gates and partially turned-on pass gate transistor in the logic and memory circuities respectively. In Section 2, we studied the dependency on the states of the non-failing inputs for the generation of defect-induced emission on various combinational logic gates. The differences in emission signatures between open and short defect are then discussed and utilized to identify the defect type and location in subsequent case studies. Section 3 describes the localization of opens and shorts through the induced emission from the affected wordline node of the pass-gate transistors. The last section discusses on the limitation of such approach and highlights the critical factors for the applications on more advanced technology nodes devices.

2. Localization of open & short defects in logic

One of the most challenging types of yield limiting defects is resistive open and short defects that fall along or between dense metallization signal nets in the logic circuitry. Fig. 1 (a) and (b) illustrates the example of a resistive bridging defect, R_{defect} that falls between the power supply and ground, and between 2 inverters' signal output paths respectively. While the bridge between V_{DD} and V_{ss} would result in a short or leakage and possibly be drawing sufficiently high current density, I_{leak} for easy defect localization with TIVA or OBIRCH, a bridge between 2 signal paths may yield marginal or no leakage. A small leakage, i_{leak}, would flow only if input A and B are of different logic states (i.e. A is HIGH and B is LOW or vice versa). Moreover, since i_{leak} is limited by the technology dependent transistors' drive current, the defect current density is restricted and this degrades detection sensitivity. Thus, these subtle defects are hard to localize and they would result in logic or analogue [18] functional failures where the functional mode cannot be easily triggered by reduced 2 pin power (V_{DD}) to ground (V_{ss}) biasing for static fault localization techniques. Even if hotspots could be detected from these techniques, the hotspots are typically symptoms of the defect instead of pointing to the defect locations. Conventional PFA approaches of top down delayering or progressive Focused Ion Beam (FIB) cross-sectioning at the hotspot locations would be futile in observing the physical defect. To increase the probability of finding the defect, PFA has to encompass a larger inspection area or in the case of finding a suspected open via/contact, perform a tedious larger area Passive Voltage Contrast (PVC) comparison between good and bad unit. This approach is made even less effective with the increasing challenge of achieving large area planarity for top down layer by layer de-processing for advanced technology nodes beyond 65 nm.

2.1. Characterization of combinational logic responses to shorted or floating input

The effects of a defect resulting in a shorted or floating gate input along a signal path in the logic circuitry was studied on standard combinational logic test structures that were fabricated on 40 nm process. From these learnings, differences in the defect induced emission signatures between a short and open defect were deduced. These characteristic signatures were effective in predicting the type of defect. For open defect, a novel method is also derived to narrow down the potential open defect location from the entire signal failure path into a much smaller segment. This approach is applied with great success to localize open and short defects resulting in yield loss from advanced technology nodes, with significant reduction in FA cycle time.

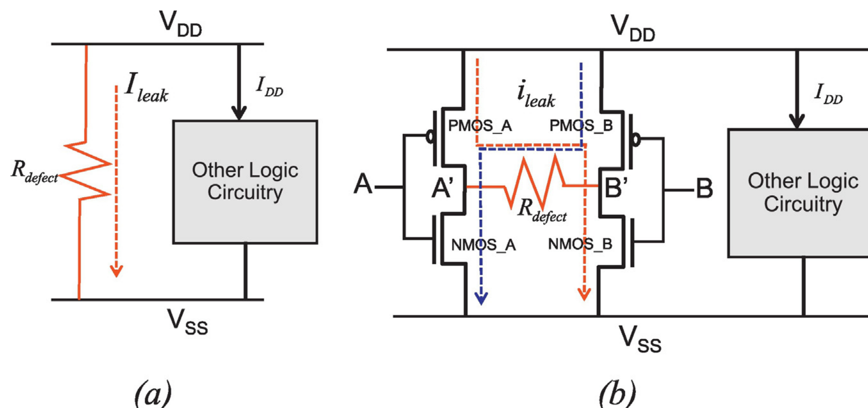

Fig. 1. Simplified circuits to illustrate a bridging defect (a) between power supply to ground and (b) between 2 logic signal paths.

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