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Highly reliable and low-power magnetic full-adder designs for nanoscale technologies

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ABSTRACT

The MTJ-based circuits have been considered as a candidate for next generation digital integrated circuits thanks to their attractive features such as nonvolatility, low leakage current, high endurance, and CMOS integration compatibility. However, incurred energy and delay by reconfiguration of their employed conventional MTJs limit their application. Besides, the issue of read-disturbance is another challenge in such MTJ-based circuit designs. In this article, a new magnetic-based full-adder (MFA) circuit based on a new three-terminal two-in-one magnetic tunnel junction (TIO-MTJ) cell is proposed. Comparing with the previous MFA circuits, the proposed circuit offers a lower energy for the write operation and also a disturbance-free reading. Two improved structures based on the proposed MFA are also suggested to obtain the advantages of nonvolatility for the power-gating architectures and also radiation hardening for the radiation harsh environments.

1. Introduction

Magnetic-based random access memory (MRAM) is widely taken into consideration thanks to its distinctive attributes such as nonvolatility, low leakage current, easy integration with CMOS technology, and high performance [1–3]. The basic and key element of magnetic logic is magnetic tunnel junction (MTJ). Conventional MTJs are comprised of three layers including two ferromagnetic (FM) and one thin oxide layers [1–3]. Fig. 1.a shows the conventional MTJ structure. As shown in this figure, the FM layers (sandwiching the oxide layer) are in free and pinned forms. As there are two possible modes including parallel and antiparallel for the FM layers, MTJ can show two different resistances in these modes. The resistance associated with the parallel mode (R_P) is lower than the one for the antiparallel mode (R_{AP}) [2,3].

To reconfigure the MTJs, there are a number of writing mechanisms that the spin transfer torque (STT) [5] is currently the most widely used thanks to its lower delay and energy consumption [6,7] than its prior counterparts. However, the STT-MRAMs are still suffered from a considerable energy and also delay for the write operation [7]. This issue limits their application and includes performance challenge for design of very high-speed and low-cost memories such as level-1 cache memories [7,8]. Another serious challenge in STT-MRAMs with the conventional MTJs is the read-disturbance issue [8]. As there is a common path for both the write and read currents, there is a possibility of data flip during a read operation. In other words, it is possible that the read current results in an unwelcome reconfiguration of the MTJs [7,8].

Fig. 1.b shows a 3-terminal, 5-layer MTJ structure that can act as two conventional MTJs [7]. In this paper, this MTJ type is called two-in-one MTJ (TIO-MTJ). As shown in Fig. 1.b, the TIO-MTJ is comprised of five layers including three FM layers and two oxide layers isolating the FM layers. The upper and lower FM layers are fixed, and the middle FM layer is free [7]. As the fixed layers are in opposite direction, the free layer always agrees with one of the fixed FM layers and disagrees with the other one [7–9]. Therefore, there are two possible modes based on the free layer direction. It is discussed in [7] that, the TIO-MTJ needs less current for reconfiguration resulting lower energy consumption for the write operation. The reasoning is that this MTJ needs only one FM layer reconfiguring to obtain two changes in parallel/antiparallel states while the conventional MTJs need reconfiguration for two free FM layers to change two parallel/antiparallel states [7,8]. In [7], it is also shown that their proposed TIO-MTJ provides a disturbance-free read operation as well as high tolerance to process variation (higher than the conventional MTJs [7]). The fabrication process of the TIO-MTJ is similar to the conventional MTJs. Therefore, similar to the conventional MTJ, the TIO-MTJ has an easy integration with the CMOS technology [1,7–9].

A typical magnetic logic circuit has two modes including evaluate (read) and pre-charge (write). During the evaluation mode, a CMOS circuit, the sense amplifier (SA) circuit, senses the MTJ states and during the pre-charge state a CMOS circuit (the write circuit) reconfigures the MTJs based on input signals. When one of the SA/write circuits are active in the related mode, the other one is bypassed.

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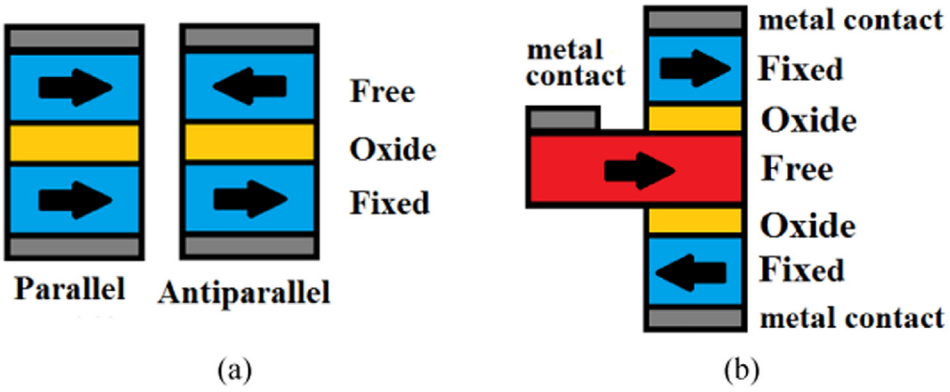

Fig. 1. Magnetic tunnel junction (MTJ): a) conventional 2-terminal, 3-layer MTJ b) TIO-MTJ including 3-terminal and 5 layers [7].

In this paper, we propose a new single-MTJ magnetic full-adder (SMFA) circuit based on the TIO-MTJ. Over the previous work, this circuit offers a lower power consumption as well as a higher readability. Also, two extensions of the proposed SMFA including a fully nonvolatile (NVMFA) and a fully radiation immune (RHMFA) are suggested and evaluated. Increasing in sensitivity to radiation effects are of concerning reliability issues in today's CMOS circuits [3,6].

The rest of this paper is organized as follows. The next section reviews previous magnetic full-adder (MFA) circuits. Section 3 presents our proposed TIO-based MFA circuits. The fourth section provides simulation results and discusses the advantages offered by the proposed MFA circuits. The last section concludes the paper.

2. Motivation and previous work

Following scaling down of CMOS technology, leakage power increases dramatically [10,11]. In fact, every path between V_{DD} (the supply voltage) and GND (the ground) can result in leakage current. Locating an MTJ cell in such paths can reduce the leakage current significantly [2]. Also, increasing susceptibility to radiation effects by shrinking in CMOS dimension is another issue in CMOS circuit design. Energetic particles striking an off-state transistor could affect a memory/sequential logic circuit and result in a soft error that is called single event upset (SEU) [12]. SEU is the phenomenon of logic altering stored in a sequential logic due to a particle strike [12].

MTJ-based circuits can offer various advantages including low standby power and nonvolatility [2–4]. Heretofore, various MTJ-based memory and logic circuits are proposed by the literature. In [2,13–16], various MFA circuits are suggested. As an example, the proposed circuits in [2,14] include four conventional MTJ cells, a CMOS circuit for write, another for read and a CMOS logic tree (LT). In fact, these circuits have a logic-in-memory architecture [2]. The later uses the dynamic logic approach that has two modes of pre-charge and evaluation [2,3]. Generally, in such architectures, the logic tree (LT) component (denoted in Fig. 2) computes a specific logic function and along with the SA circuit (Fig. 2) results in both output and its complementary logic. Proposed MFA in [2] saves input B by the MTJ cells, while the other inputs of A and Ci are volatile. In [13], for inputs of A and Ci, an MTJ-based memory element is considered to give the MFA circuit nonvolatility. In [15], a similar approach for full-nonvolatility is suggested (based on the conventional MTJ). In [16], another full nonvolatile MFA is suggested. Their suggested MFA uses an MTJ-pair for every input of A, B, and Ci. In other words, for both circuits of summation (SUM) and carry-out (Co), a total of 16 conventional MTJs is employed. This circuit offers a zero leakage current as well as full nonvolatility. However, as compared with the conventional CMOS-based FAs, this circuit incurs more delay [16]. Also, in comparison with the MFAs suggested in [2,14], a higher energy for write is needed by this circuit [7,8]. In [14], another MFA circuit with a similar idea with [2] is proposed.

All the considered previous MFA circuits are based on the conventional MTJ cells (Fig. 1.a) that need a high energy for the write operation [8,9]. Also, these circuits suffer from an important issue of read-disturbance and also sensitivity to radiation effects in their sequential CMOS sub-circuit [7–9].

The next section proposes a new MFA circuit based on the TIO-MTJ cell. This circuit is then enhanced to achieve full-nonvolatility to be used in nonvolatile integrated circuit (IC) designs for nonvolatile computing. Besides, the issue of radiation hardening is taken into consideration and a radiation hardened version of the proposed MFA is proposed. Comparing with conventional MFAs, our circuit needs fewer

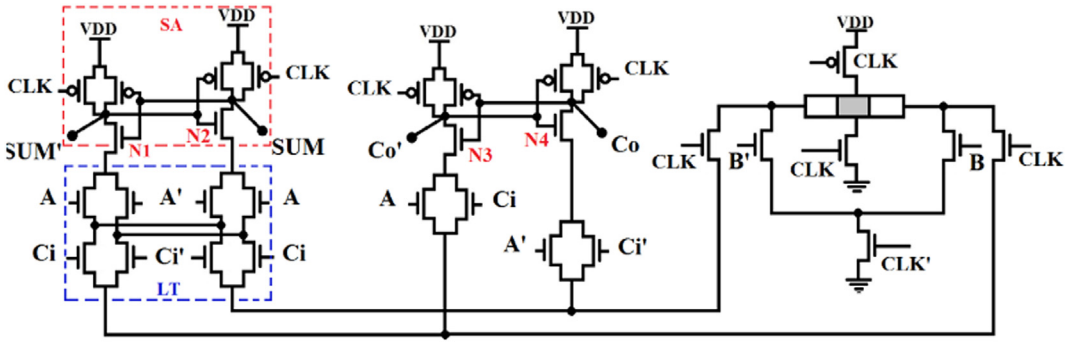

Fig. 2. Proposed single-MTJ MFA (SMFA).