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Research paper

SEU reduction effectiveness of common centroid layout in differential latch at 130-nm CMOS technology

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ABSTRACT

In this paper, we apply the common centroid layout technique in a differential latch structure (i.e., Quatro) and evaluate its effectiveness in reducing single event upset vulnerability. SPICE simulations demonstrate that higher charge sharing efficiency between the differential pair of sensitive devices results in higher critical charge of the latch. Both regular and common centroid layouts show the same heavy ion upset Linear Energy Transfer (LET) threshold because this is determined by the worst case critical charge (i.e., there is no charge sharing). Additionally, the magnitude decrease in the cross section of common centroid layout than that of the regular layout is not significant in 130-nm CMOS bulk technology because cross section covers the highest charge sharing efficiency and the lowest charge sharing efficiency from statistical point of view.

1. Introduction

Single event upsets (SEUs) induced by radiation strikes may disrupt the function of electronic systems [1,2,3]. In the International Technology Roadmap for Semiconductors (ITRS) reports, these errors have been identified as major challenges [4]. SEUs can be mitigated through a variety of techniques at different levels. Triple Modular Redundancy (TMR) and Error Checking Code (ECC) are widely used at the architectural level [5]. However, they incur significant power, area, and speed penalty; and thus, this renders them unattractive for constraint applications. Instead, SEU-hardened storage cells, such as DICE [6], Quatro [7] and their variants, are preferred by ASIC designers. These designs, more or less, take advantage of spatial or temporal redundancy.

As Moore's law predicts, the feature size of ICs scales down. This leads to smaller inter-device spacing and nodal capacitance, which is translated to higher density of devices, faster speed, and smaller power consumption. In the meantime, these technology advances result in increasingly significant charge sharing (i.e., multiple node charge collection due to a single particle strike). In our paper, charge sharing efficiency ∅ is defined as the ratio of the charge collected by the secondary node vs. the deposited charge at the struck node.

As presented and compared in [8], when the devices in a 130-nm technology are spaced 0.18 μm away, the passive PMOS collects ~5% of the deposited charge on the active PMOS for a particle LET of 10 MeV*cm^2/mg. Thus, ∅ is 5% in this case. Yet in another case of LET = 30 MeV*cm^2/mg, ∅ significantly increases to ~30%. It is also expected that as the LET increases, ∅ will significantly increases as well.

Charge sharing efficiency also strongly depends on the layout parameters, i.e., the well resistance (*R_well*) as well as the vertical contact resistance (*R_contact*), as shown in Fig. 1. *R_well* is given by $R\_well = \rho^* L/(W^* H)$, where ρ is the resistivity of the well, H is well depth, W is well width, and L is the spacing between the device and well contact. TCAD simulation results in [8] demonstrate that as the spacing L varies from 1.62 μm to 0.18 μm, ∅ increases by ~5× for PMOS devices, while ∅ increases by ~15× for NMOS devices.

As a consequence, circuits of the same design tend to present higher sensitivity in advanced technology nodes. DICE, a design virtually immune to single node upset, may collect charge on multiple nodes due to charge sharing and consequently upset, even if only a single node is hit [9].

Researchers in the radiation effects community have turned their attention to layout-level hardening techniques in the past decade. Separating sensitive nodes in the physical dimension has proven to be effective in reducing charge sharing and increasing SET/SEU tolerance, albeit it increases the layout area [8,10]. Adding well/substrate contacts helps in maintaining well/substrate potential and channel excess carriers through the supply rail [11,12]. Lee and Lilja et al. have proposed and experimentally verified LEAP - a technique of intelligent placement of devices to combat charge sharing in multiple technology nodes [13,

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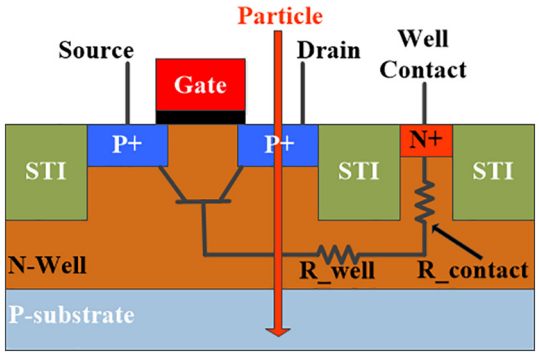

Fig. 1. The structure of the parasitic bipolar transistor and the resistances (*R_well* and *R_contact*) that affect well potential and charge sharing.

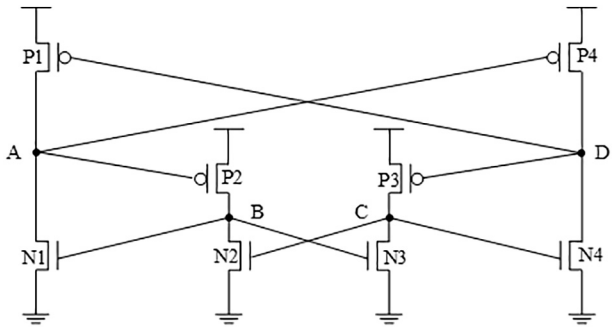

Fig. 2. The structure of Quatro presented in [7]. It features four storage nodes (A, B, C, and D) and two differential structures. One is formed by P2/N2 and P3/N3; the other one is formed by P1/N1 and P4/N4.

14]. Lilja invents a unique layout method to harden logic cells through a rearrangement of critical sensitive nodes [15].

The common centroid layout technique has been used and investigated for differential analog circuits, such as current amplifiers [16,17]. For the switched-capacitor sample-and-hold amplifier fabricated on a 130-nm CMOS technology, the common centroid structure reduces the cross-section by approximately 1.5× than its regular layout counterpart [16]. However, to the authors' best knowledge, no one has ever applied this technique on digital latch design and evaluated its effectiveness. As Quatro, by its very nature, is a differential structure, we simulate and experimentally evaluate its design variant by applying the common centroid layout technique.

The rest of the paper is organized as follows: Section 2 reviews Quatro's structure and single node upset issue. Section 3 demonstrates the structure of the Quatro design variant utilizing the common centroid layout technique and the simulation results. Section 4 presents the test chip design and testing system setup. The heavy ion data and analysis are given in Section 5. Section 6 concludes the work.

2. Background

The conventional D latch or 6T SRAM cell consists of a pair of inverters forming a positive feedback loop. Clearly, this type of structures has two storage nodes; and they store the true and complement values. An SET glitch on any node induced by a radiation strike may propagate to the opposite node through the feedback path and consequently flip the cell.

Quatro is an SEU-tolerant latch that has redundant storage nodes, as illustrated in Fig. 2. Quatro has proven to be more power and area efficient than DICE [7] and manifests to be an alternative to DICE. Similar to DICE, it has four storage nodes named A, B, C and D in this text. Two of them store the true value, while the other two store the complement value. If a single node is hit, the other nodes will try to recover their states and maintain the logic values of the cell.

However, as noted by the authors, Quatro is not immune to single node strikes [7]. A positive SET glitch on node B or C may still cause erroneous upsets. This issue is illustrated and explained as follows.

Assume that nodes A, B, C, and D hold logic 1, 0, 1, and 0 respectively. If node B observes a 0 ⟶ 1 SET glitch after a particle strikes this node's pull-up transistor P2, this SET transient will likely turn on N1 and N3 simultaneously. They will then pull down the node voltages of A and C, followed by flipping node D.

The positive SET glitch is simulated by injecting a double-exponential current source onto node B, whose rise and fall time are 50 ps and 200 ps respectively. Quatro flips when the deposited charge is 100 fC. Therefore, node B is sensitive in this case. Similarly, node C is sensitive when nodes A, B, C, and D hold logic 0, 1, 0, and 1, respectively.

3. Common centroid layout technique and its application in Quatro

3.1. Common centroid layout technique

Fig. 3 compares the ways of laying out transistors in ASIC designs. The traditional way of placing transistors in the layout is to position the source and drain regions on both sides of the polysilicon gate and aligning them horizontally, as illustrated in Fig. 3(a). This figure shows how P1 through P4 and N1 through N4 are laid out as our reference layout style for Quatro.

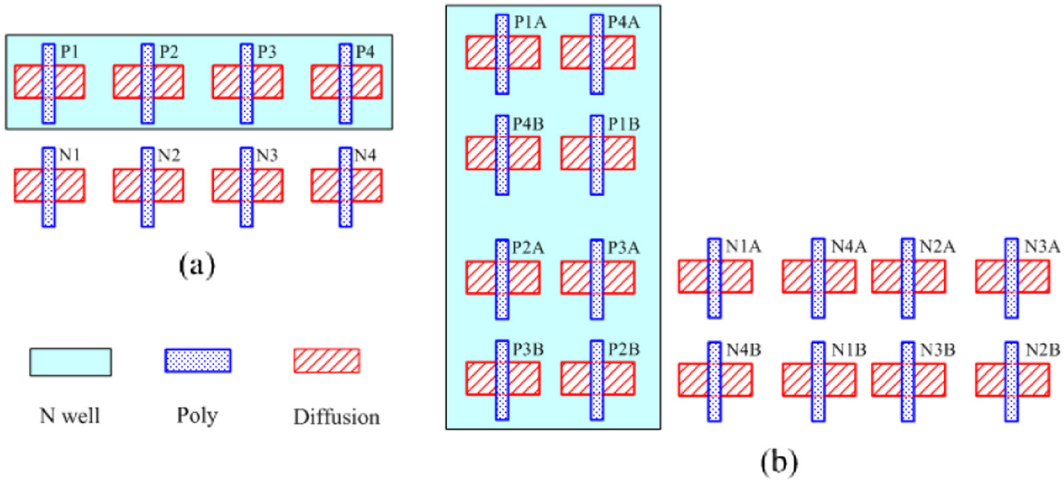

Fig. 3. Two layout variants of Quatro: (a) the traditional layout style; (b) the common centroid layout style.