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Influences of silicon-rich shallow trench isolation on total ionizing dose hardening and gate oxide integrity in a 130 nm partially depleted SOI CMOS technology

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ABSTRACT

The influences of silicon-rich shallow trench isolation (STI) on total ionizing dose (TID) hardening and gate oxide integrity (GOI) in a 130 nm partially depleted silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technology are investigated. Radiation-induced charges buildup in STI oxide can invert the parasitic sidewall channel of the n-channel transistor, which will increase the off-state leakage current and decrease the threshold voltage for the main transistor. Compared with the general STI process, the silicon-rich STI process can significantly suppress the increase in leakage current and negative shifts in subthreshold region induced by the total dose radiation, implying TID hardening for STI trench oxide. However, the silicon-rich STI process has a deleterious impact on GOI. It leads to the thin gate oxide thickness at trench corner and lowers the gate oxide breakdown voltage. Issues of gate oxide integrity induced by silicon-rich STI are investigated in this paper, and an optimized process to solve this problem is proposed and examined. Finally, the TID response of the optimized silicon-rich STI process is presented in comparison to the general and silicon-rich STI processes.

1. Introduction

With the development of military and space electronics technology, the total ionizing dose (TID) radiation effects and hardening of metal-oxide-semiconductor (MOS) technology have been concerned and investigated during the past fifty years. The TID effects due to the accumulation of ionizing radiation over time result in long-term degradation in device performance. It is well known that electron-hole-pairs (ehps) are generated in gate and isolation oxides during irradiation [1,2]. The electrons, having a much higher mobility than holes in oxides, are rapidly swept out of the oxide [3], whereas the surviving holes fall into deep traps in the oxide bulk or near the Si/SiO_2 interface, which forms the trapped positive charges. These fixed oxide trapped charges N_{ot} result in a negative shift in the transfer characteristic curves of n-channel MOSFETs, and lead to a reduction in threshold voltage and an increase in off-state leakage current [4–8]. As the gate oxides of deep submicron CMOS technologies are scaled to thinner dimension, the threat of shifts in dc parameters due to N_{ot} buildup in the gate oxide is reduced [9,10]. However, the shallow trench isolation (STI) trenches are not scaled for advanced CMOS technologies. The typical thicknesses of STI ranged from 300 to 450 nm are much thicker than gate oxides, which now becomes a greater radiation threat and the most important focus for total dose radiation hardening in modern CMOS technologies [11,12].

To improve the radiation hardness of STI, many special procedures have been proposed and investigated in the past years. They mainly can be divided into two categories. One category is new layout approach. By pulling back the source and drain regions from the trench edges [11] or using enclosed layout transistors (ELT) [13], the new layouts can effectively suppress or completely eliminate the parasitic leakage path. However, the drawbacks of changing layout become evident when manufacturing complex high density ICs, due to the limit W/L ratio and increasing chip area of ELT. The other category is process optimizing. It was discovered that implanting aluminum and silicon in the oxides could introduce electron traps or nanoclusters (both trap negative charges) compensating the hole traps [14,15]. Some works also found that fluorinated oxides [16] or nitride oxides [17] improved the radiation hardness. Instead of the single layer dielectric film of a

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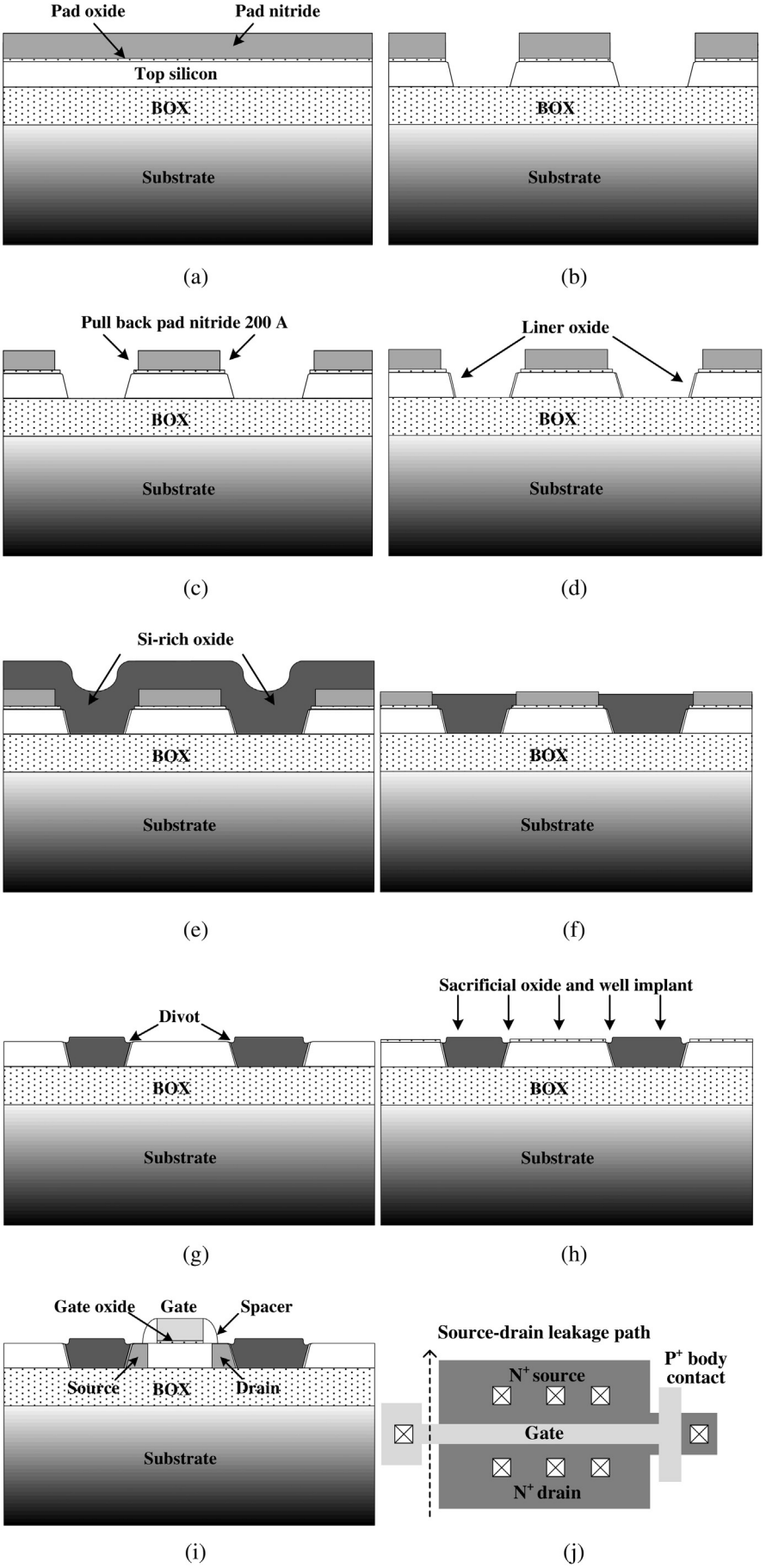
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Pad nitride
Top silicon
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Substrate
(a)
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(b)
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Liner oxide
BOX
Substrate
(d)
Si-rich oxide
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Substrate
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N+ drain
P+ body contact
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