

Impact of gate-to-source/drain misalignments on source-side injection Schottky barrier charge-trapping memory cells evaluated using numerical programming-trapping iterations

Chun-Hsing Shih ^{a,*}, Yen-Hsiang Lo ^b, Yu-Hsuan Chen ^{a,b}, Jr-Jie Tsai ^a

^a Department of Electrical Engineering, National Chi Nan University, Nantou 54561, Taiwan

^b Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

ARTICLE INFO

Article history:

Received 24 November 2016

Received in revised form 19 March 2017

Accepted 26 April 2017

Available online xxxx

Keywords:

Gate-to-source/drain misalignments

Schottky barriers

Source-side injection

Charge-trapping memory

ABSTRACT

This work numerically elucidates the effects of gate-to-source/drain misalignments on source-side injection Schottky barrier charge-trapping memory cells. The coupling of Schottky barriers and trap charges generate particular Schottky barrier lowering and source-side injection, while the charge-coupled Schottky barriers must be considered concurrently with the precise positions of metallic source/drain junctions. Numerical programming-trapping iterations were employed to examine the distribution of electron injections and trapped charges in the charge-coupled cells, and to discuss the differences of physical mechanisms among the aligned, overlapped, and underlapped cells. The overlapped cells produce a mildly high programming and reading currents because of the shorter effective lengths. However, the underlapped cells suffer severely from the degradation of electron drain current, hot-carriers injection, and threshold-voltage shift because of widened tunneling barrier, reduced electric field, and invalid injection location. Mildly gate-to-source/drain overlap should be designed in Schottky barrier charge-trapping memories to avoid the underlapped offsets, ensuring favorable programming and reading performance.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

Metallic Schottky barrier source/drain has been intensively studied because of their potentiality to minimize resistance, serving as attracting alternatives in semiconductor industry [1–8]. Because the Schottky barrier junctions can produce a strong enhancement of hot-carriers generation to ensure a large gate current at low voltages [9–11], Schottky barrier source/drain was employed in nonvolatile charge-trapping memories to exhibit unique source-side programming [10–12]. Their excellent injection and cell characteristics were experimentally and numerically verified [11–15]. However, it is very difficult to ensure fully-aligned Schottky barrier source/drain devices in practice. The misalignments strongly affect the device characteristics [1,16–18]. For the Schottky barrier charge-trapping cells, the Schottky barrier tunneling and source-side injection rely highly on the actual Schottky barrier profiles, the gate-to-source/drain offsets must be concurrently considered. Whether a misaligned profile can be used, or what kinds of alignments should be utilized to ensure favorable cell reading and programming.

Conventionally, self-aligned silicide (salicide) was employed to fabricate doped source/drain in CMOS devices [19–22]. The precise position

of doped junctions was controlled by the self-aligned implantation and the spacer formation. To be compatible with CMOS technologies, the fabrication of metallic Schottky barrier source/drain was modified from the conventional salicide process [1,23]. For fabricating metallic source/drain, metal deposition and subsequent thermal annealing was performed after the sidewall spacer. The actual position of metallic Schottky barrier junctions relies on the sophisticated silicidation steps and structural device parameters. Thus, it is hard to achieve fully-aligned Schottky barrier cells in practice. Because the practical Schottky barrier profiles play the key roles in determining the Schottky barrier tunneling and source-side electron injection, complete discussion of the impacts of gate-to-source/drain offsets on cell reading and programming characteristics is crucially required. But, those parts were not considered previously.

This work elucidates the effects of gate-to-source/drain misalignments on source-side injection Schottky barrier charge-trapping cells. Successive injection-trapping iteration processes were used in Schottky barrier cells to study the coupling of the trapped charges and the misaligned Schottky barrier lowering during cell programming [15], and to examine the differences of programming and reading mechanisms between the aligned and misaligned Schottky barrier cells. Because the precise variations of gate-to-source/drain offsets can be generated in numerical simulations, this study employed two-dimensional device simulations [24] to investigate the cell characteristics

* Corresponding author.

E-mail address: shihch@ncnu.edu.tw (C.-H. Shih).

with various overlapped and underlapped gate offsets. Section 2 details the cell structures and physical parameters used in numerical simulations. Section 3 explores the effects of gate-to-source/drain alignments on electron drain current and source-side injection programming. Section 4 discusses the numerical results of cell programming and reading of aligned and misaligned Schottky barrier cells using successive injection-trapping iterations.

2. Device structures and physical parameters

Fig. 1 depicts the schematic structure of aligned, overlapped, and underlapped Schottky barrier charge-trapping cells used in numerical simulations. A typical silicon-oxide-nitride-oxide-silicon structure was employed in the Schottky barrier cells, where the multi oxide/nitride/oxide layers of 5/6/7 nm were used to represent the charge-trapping dielectric layers. The gate-to-source/drain offsets of 5/10/15 nm were employed in the overlapped or underlapped Schottky barrier cells to study the effects of gate-to-source/drain misalignments caused by the modified salicide approach [1,19–22]. A long-channel 180 nm cell with uniform profile was utilized to focus on studying the inherent cell characteristics without the disturbance of sophisticated profiles and short-channel effects. A midgap workfunction gate and a junction depth of 50 nm were employed with a uniform p-type substrate of $1 \times 10^{17} \text{ cm}^{-3}$.

To study the effects of Schottky barriers on cell devices, numerical simulations were performed using the thermionic emission and Wentzel-Kramers-Brillouin-based tunneling models [12,25,26]. The detail discussion of physical models used in the numerical simulations can be found in Ref. [12]. An electron Schottky barrier height of 0.4 eV was employed in metallic source/drain to represent the conventional workfunction using CMOS technologies [1,19–22]. The lowering of Schottky barriers by the image force and dipole effect was considered to determine the effective Schottky barrier heights [12,27,28]. To evaluate the characteristics of source-side electron injection, the impact ionization, lucky-electron, and band-to-band tunneling models were employed to predict the injected gate currents [29–32].

3. Effects of misalignments on Schottky barrier cells

3.1. Ambipolar conduction and drain current

Fig. 2 shows the typical current-voltage curves of aligned, overlapped, and underlapped Schottky barrier cells, in which the misaligned gate-to-source/drain offsets of 15 nm were used. The ambipolar conduction of Schottky barrier cell devices depend strongly on the gate-to-source/drain misalignments. Notably, the overlapped offset produces a mild effect on the current-voltage characteristics of Schottky barrier

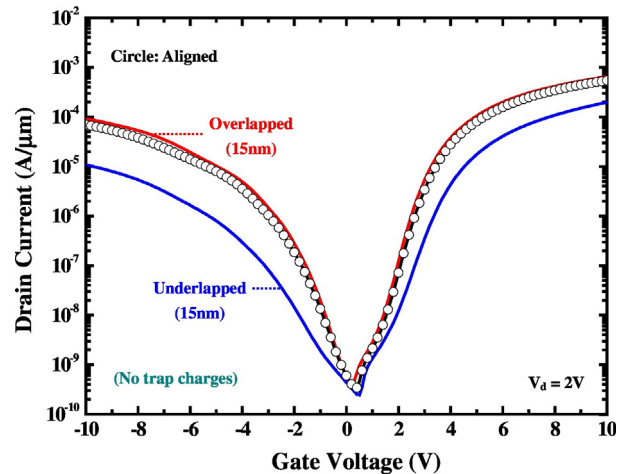


Fig. 2. Ambipolar conduction of aligned, overlapped, and underlapped Schottky barrier charge-trapping cells, in which misaligned offsets of 15 nm were used.

cells to increase both the electron and hole currents, whereas the underlapped misalignment causes a substantial reduction of on-state electron current and ambipolar off-hole current in Schottky barrier cell devices.

Because the electron current was employed for cell programming and reading, Fig. 3(a) and (b) respectively present the electron drain

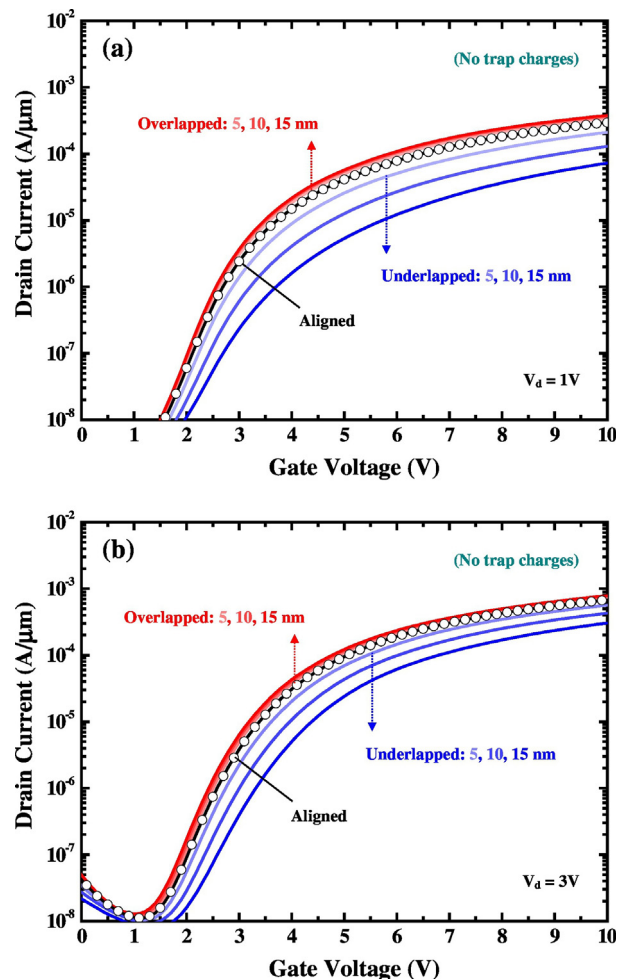


Fig. 3. Effects of misalignments on electron drain currents of fresh Schottky barrier charge-trapping cells at (a) $V_d = 1 \text{ V}$ for cell reading, and (b) $V_d = 3 \text{ V}$ for cell programming.

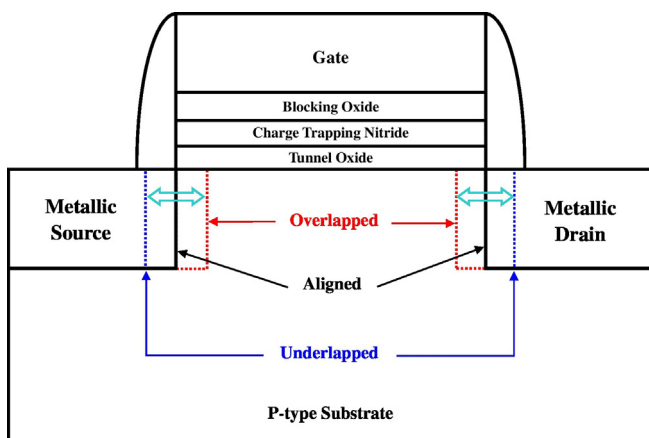


Fig. 1. Schematic structure of a fully-aligned, underlapped, or overlapped Schottky barrier charge-trapping memory cell.

Download English Version:

<https://daneshyari.com/en/article/4971545>

Download Persian Version:

<https://daneshyari.com/article/4971545>

[Daneshyari.com](https://daneshyari.com)