Microelectronics Reliability 74 (2017) 34–43

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory invited paper

# Experimental and numerical study of 3D stacked dies under forced air cooling and water immersion cooling

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ARTICLE INFO

*Article history:*
Received 8 October 2016
Received in revised form 17 January 2017
Accepted 22 February 2017
Available online xxxx

*Keywords:*
3D stacked dies
Forced air cooling
Water immersion cooling
Heat dissipation ability
Thermal management

ABSTRACT

3D stacked die structure is a promising architecture to realize small feature size and enhance electronic performance. However, thermal performance in 3D stacked die has aroused extensive attention for its high density integration. In this paper, a stacked dummy die structure integrated with polyimide heater inside is presented to investigate the thermal behavior of 3D stacked dies. One-dimensional thermal resistance network is built and calculated to analyze thermal resistance distribution of the stacked dies. Under natural convection, the thermal resistance of convective heat transfer greatly influences total thermal resistance and limits heat dissipation ability of stacked dies. To significantly reduce the thermal resistance of convective heat transfer, forced air cooling and water immersion cooling have been applied in the stacked die structure. Experiment and numerical simulation have been conducted in this work. In the experiment, forced air cooling and water immersion cooling systems are set up to cool down the stacked die structure. The temperature dependence of the stacked die structure is obtained by thermocouples. The measured thermal resistances between junction and ambient environment of the stacked die structure decrease to 7.6 °C/W under forced air cooling and to 0.6 °C/W under water immersion cooling, respectively. Then heat dissipation abilities of forced convection cooling for the stacked die structure are analyzed. Simulation models are built for experimental validation and further thermal analysis. Temperature influences on the internal structure of the stacked dies with different power map are discussed. The simulation results can well capture the experimental results with 5.8% variation under forced air cooling and with 7.4% variation under water immersion cooling when total power of 3 W is applied.



## 1. Introduction

Since nearing the physical limits to CMOS scaling, the increasing of transistor density becomes increasingly difficult. With the progress in package and interconnection technology, the innovation of 3D integration becomes essential to extending the Moore's law [1–4]. Compared with the plane assembly configuration, the 3D integration by stacking chips in vertical direction greatly reduces the assembly size. Interconnects between vertical dies are potential much shorter than a 2D assembly, allowing for higher signal speed and smaller power consumption. The 3D stacked dies enable to integrate various function chips in different layers. Each layer in the stack can be a sub-system [3]. Since different function chips is manufactured separately, good dies can be known before 3D assembly. It offers the possibility of high yields and hence reduces cost than other system integration configuration, system on chip (SOC) for example [4].

However, as stacking chips in vertical direction, it complicates the thermal behavior with multiple power dissipation interaction. Power dissipation becomes exacerbated as power density increases linearly with the number of dies stacked. In the case of ultra-thin stacked dies, the increase of horizontal heat resistance makes it more difficult to conduct the heat from hot spot to peripherals. The thermal behavior of the 3D stacked die has been studied by many researchers. Keiji Matsumoto studied the equivalent thermal conductivity of the interconnection and hence determined the connection thermal resistance of the 3D stacked chips [5]. John H. Lau studied the effects of the TSVs on thermal performance of 3D IC. The junction temperature and thermal resistance of 3D IC with various TSV interposers have been determined [6]. New material with high thermal conductivity just like graphite sheet is also proposed to spread hot spots heat [7].

Thermal models of the 3D stacked chips, including numerical models and analytical models, have been developed with considering calculation accuracy and computation efficiency. The finite element models of the 3D stacked chips are proposed for obtaining detailed temperature distribution [8]. However, these models have to sacrifice much computer resource and computation speed, especially in transient thermal

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http://dx.doi.org/10.1016/j.microrel.2017.02.016
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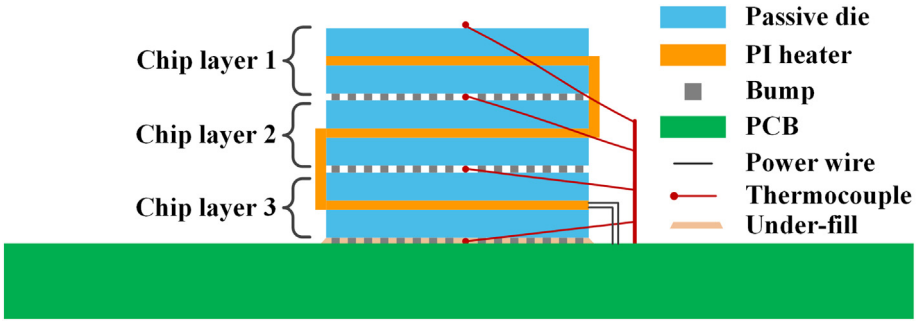


**Fig. 1.** The schematic of the 3D stacked dies.

analysis. The one-dimensional thermal resistance network models offer a fast and simple method for approximate junction temperature prediction, in particular in the case of uniform heating dies [9,10]. Compared with the 1D thermal resistance models, Leila Choobineh developed a sensitive 3D heat transfer model for the 3D stacked dies based on Fourier series expansion and Laplace transforms. Accurate layer temperature profile and hot spots distribution have been obtained through complex iterative calculation [11].

Thermal dissipation approaches have been investigated for cooling different power density 3D stacked dies. Under the air cooling, thermal performance of the 3D stacked dies numerical model with one high power processor integrated with 4 memory dies can hardly be handle unless large heatsink and higher air velocity are applied [12]. Instead, microfluidic cooling attracts tremendous attention for cooling the next generation 3D system. The silicon interposer with micro pin fin array was integrated in the 3D stacked dies, which achieved a lower thermal resistance of convective heat transfer [13–15]. IBM developed the inter-tier liquid cooling of the 3D ICs. Performances of inter-tier cooling including pressure drop and heat dissipation ability were investigated. The maximum heat removal performance was achieved >200 W/cm$^2$ with 0.6 × 10$^5$ Pa pressure drop [16]. However, the thermal performance of 3D stacked dies under liquid immersion cooling has not been extensively studied. Under liquid immersion cooling, it needs to protect stacked dies against mechanical stress, corrosion and electrical short circuit with careful thermal-mechanical design.

In this paper, we study not only the numerical models but also experiments on forced air cooling and water immersion cooling for the 3D stacked dies. A 3D stacked die structure with three chip layers is designed and constructed. In the stacked die structure, a flexible polyimide heater is integrated inside to act as dies heating. The connection of each chip layer is achieved by bumps to pads flip-chip bonding. Ultrathin thermocouples are stretched into the middle of the bump area to obtained layer temperature. Thermal resistance distribution of the stacked die structure with PCB and heat sink is studied by one-dimensional thermal resistance network. Experiments and simulations including natural convection, forced air cooling and water immersion cooling are built. Under different cooling methods, the temperature profiles of the stacked die structure are carefully discussed. The cooling capacity of forced convection cooling for the 3D stacked die structure is analyzed.

## 2. 3D stacked die structure

### 2.1. 3D stacked die construction

To investigate thermal performance of the 3D ICs, a 3D stacked die structure integrated with polyimide (PI) heater is designed and

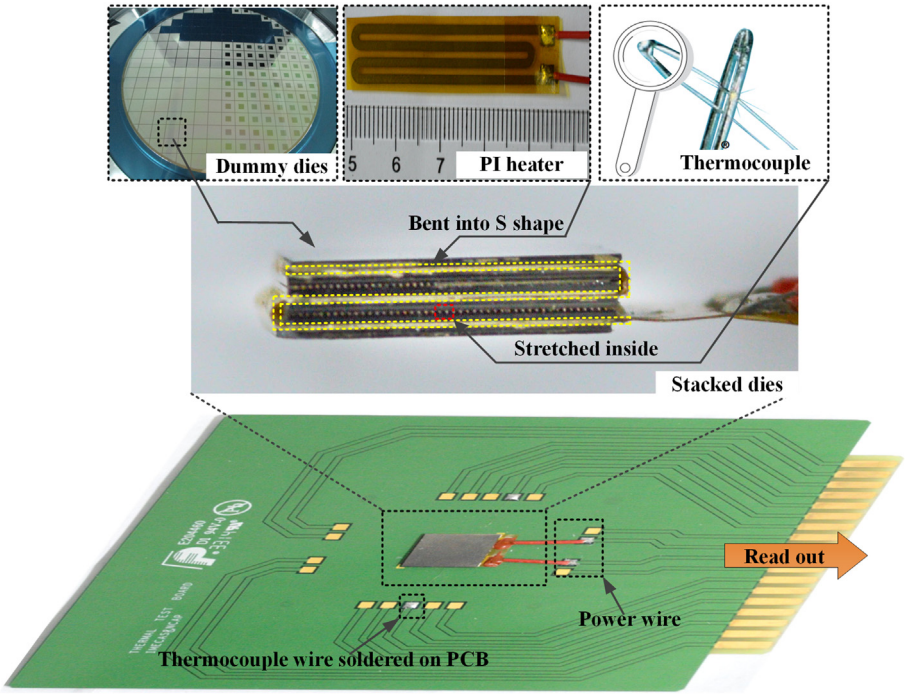


**Fig. 2.** The 3D stacked dies integration process.