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Thermal evaluation of GaN-based HEMTs with various layer sizes and structural parameters using finite-element thermal simulation☆

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ABSTRACT

By using scanning electron microscopy (SEM) and infrared data, we established and verified a two-dimensional finite-element model conforming to the size of the practical device to study high-electron-mobility transistors (HEMTs). Because the resolution of the infrared measurement was 7 μm, we verified the correctness of the model by comparing the 7-μm average peak temperature with the measured infrared data at various platform temperatures. The simulated average peak temperature agrees well with the infrared data. To further investigate the thermal performance of GaN-based HEMTs with various layer sizes and structural parameters, we simulated devices with various values of gate length, gate spacing, GaN layer thickness, substrate breadth, and substrate thickness. The conclusions presented result from some factors that must be taken into account to manage thermal issues in devices.

1. Introduction

As semiconductor device processing has advanced, AlGaN/GaN HEMTs, which have already delivered many of their promises—including high-power, high-frequency operation—in the last few years, require careful thermal management to be fully used for the exceptional power density offered by the heterostructure system [1–5]. Moreover, substantial self-heating causes a hot spot on the edge of the HEMT gate near the drain side, which negatively affects the device's performance, including its electron mobility, electron saturation velocity, and pinch-off voltage [6–12].

Clearly, the thermal design of GaN-based HEMTs is critical for their use. The channel temperature in GaN-based HEMTs can be effectively studied by physically based numerical simulations [13–17]. In early work, Eastman et al. [18] used a numerical simulation to study the gate–drain breakdown voltage and current-gain cutoff frequency (f_T) as a function of effective gate length. However, they did not show the device thermal distribution as a function of gate length. Later, Bertoluzza et al. [1], Douglas et al. [19], and Zhao et al. [20] simulated the thermal properties as the dissipated power and the device geometry. Bertoluzza et al. [1] and Douglas et al. [19] used 3D simulations to provide a much more accurate model of temperature distribution in the device. However, most of these modeled structures were highly symmetric and not based on practical device dimensions. For multifinger devices, the thermal coupling is heavily dependent on the structure of the device. Because highly symmetric structure changes the cooling conditions, in practical cases, especially for multifinger devices, highly symmetric structure is not suitable for thermal analysis. It is desired to understand the influence for thermal distribution in different structures which base on the practical structure of multifinger device.

In this paper, we establish an accurate 2D finite-element model conforming to the size of the practical device by using scanning electron microscopy (SEM) data, and we verify its accuracy by comparing it to infrared data. The simulation modeled devices with varying gate length, gate spacing, GaN layer thickness, substrate breadth, and substrate thickness, revealing results that depend on some factors that must be taken into account for proper thermal management.

2. Device description and finite-element thermal modeling

Fig. 1(a) shows the top view of the GaN-based HEMT used here, observed by laser scanning confocal microscopy (LSCM). Fig. 1(b) shows a magnified SEM micrograph of part of the device structure. Fig. 2(a) shows a cross-section of the middle position from Fig. 1(a). Fig. 2(b) shows a partial cross-sectional micrograph. Figs. 1 and 2 clearly show the device layers. The device has ten fingers. The vertical structure of the device is a 150-μm thick substrate (SiC), a 1.47-μm-thick undoped GaN layer, and a 25-nm-thick $Al_{0.3}Ga_{0.7}N$ layer. It has a gate length of 0.45 μm, gate–drain spacing of 4 μm, gate–source spacing of 2 μm, and source and drain lengths of 70 and 30 μm, respectively. The substrate

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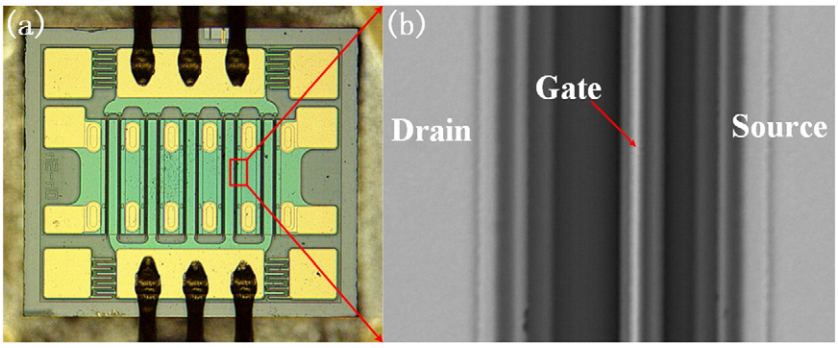

Fig. 1. (a) Top view of the GaN-based HEMT device. (b) Partial micrograph of the device structure.

breadth is 220 μm, encompassing the two sides of chip where there is no device structure, only a piece of the SiC epitaxial wafer. The model for the electrothermal simulation is based on these dimension parameters. The boundary condition for the vertical side walls of the substrate is adiabatic. The source and drain are Ohmic contacts. This model uses the following temperature-dependent thermal conductivities [21]:

$$k(\mathrm{SiC}) = 400 \times \left(\frac{300}{T}\right) \quad \left(Wm^{-1}K^{-1}\right),$$

$$k(\mathrm{GaN}) = 160 \times \left(\frac{300}{T}\right)^{1.4} \quad \left(Wm^{-1}K^{-1}\right).$$

The physically based two-dimensional numerical simulation was performed with Sentaurus Device in Sentaurus TCAD software (Synopsys Inc.). The validity of this simulation was confirmed in Refs [22,23]. To ensure the accuracy of the model, we adapted some parameters to the infrared data. The infrared measurements and simulation results were correlated using a statistical analysis.

Note that the results measured by the infrared imaging equipment are spatially averaged in areas of high heat flux because the resolution of the infrared camera at magnifications of 5× and 15× are about 7 and 3 μm, respectively. The actual heat source is less than 1 μm in width and buried under various metal and passivation layers. The averaging produces measured temperatures that are significantly lower than the actual peak channel temperature [24].

To determine whether the finite-element simulated data and infrared data correlated, the average temperature of the finite-element model was calculated across a 7-μm section centered on the heat source. If the average finite-element simulation data has an error of less than 4% when compared to the infrared data, then the model and infrared data are considered to be correlated [25]. The peak temperature of the finite-element model was used to further research the thermal properties. Fig. 3 shows the infrared image with a drain–source voltage of 28 V, drain–source current of 500 mA, and base plate temperature of 70 °C. The peak temperature spot is clearly near the gate finger, and the peak temperature is 183.73 °C. Table 1 shows the results of the 2D numerical simulation as well as the error between the simulated and measured data, revealing that the average finite-element simulated temperature coincides with the infrared data.

The electrothermal results show that the model established from the measured data is authentic and accurate.

3. Simulation results and discussion

In our model, we simulated devices with varying structural dimensions and various parameters in the device layers, from the heat source to each layer that the heat flows through.

3.1. Gate length

Because of their distinct material advantages, GaN-based HEMTs have great potential for high-frequency applications in the millimeter wavelength regime as well as for high-power applications in the microwave regime. It is important to know the speed that GaN-based HEMTs can operate, because this is the key to determining their frequency limit. With decreasing gate length, f_T monotonically increases because of decreasing gate capacitance [26–29]. Also, the temperature of the peak spot will change with changing gate length.

The models changed the gate length, ranging from 0.05 μm to 10 μm, and kept the same other parameters and electrical conditions. Fig. 4 shows the heat distribution cross section of simulation. The inset of Fig. 5 gives the channel temperature as a function of the *x*-axis with various gate lengths. This curve is obtained by cutting orthogonally along the channel shown by the red dotted line in Fig. 4. To further analyze the thermal properties from these results, we extracted the peak temperature. Fig. 5 shows the peak device temperature as a function of gate length, revealing that the peak temperature increases dramatically with gate length.

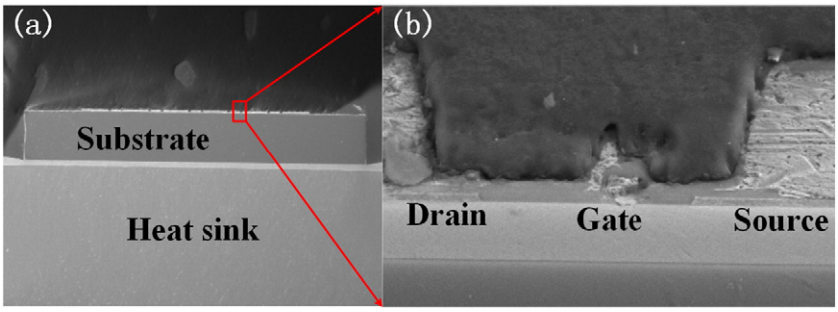

Fig. 2. (a) Cross-section of the middle position of Fig. 1(a). (b) Partial micrograph of the cross-section.