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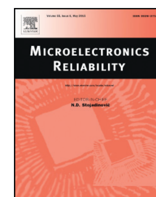

Enabling robust automotive electronic components in advanced CMOS nodes

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ABSTRACT

In this work, we have demonstrated that many elements are needed on top of conventional foundry reliability knowledge to enable robust automotive products in compliance with all restrictive norms. For intrinsic reliability, both reliability models (a design compatible WLR description), and dynamic aging compensation schemes are required. For extrinsic failures, screening procedures require well documented usage and are shown in use for volume production to bring the failure rate level down below 1 ppm automotive target. Altogether, the global approach developed in STMicroelectronics enable robust automotive products based on controlled and validated procedures.

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1. Introduction

In the last decade, automotive products have been pushed forward to advanced CMOS nodes with an accelerated pace, mostly driven by the needs for new applications like autonomous driving. In parallel, automotive markets are regulated by various norms like AEC-Q100 and/or ISO26262. Finally, the mission profiles of the products are very diverse (mostly depending on the application and its location in the car) and are generally demanding in terms of voltage and temperature excursion. On another hand, recent measurements have led the community to admit that the well-known bathtub curve is real and that the useful lifetime is shrinking down (Fig. 1) with the introduction of advanced CMOS nodes.

Reliability knowledges provided by foundry standards are limited to standard wafer level reliability (i.e. DC stress on transistors to evaluate independently the reliability mechanisms) and SRAM Test Vehicle (TV) HTOL stress (i.e. to demonstrate robust SRAM process). But these knowledges are not sufficient to build up robust automotive products. This goal requires to develop new methodologies to enable pushing the boundaries of bathtub curve (see Fig. 2).

This paper deals with the different elements and methodologies which are required to deploy on top of foundry standards in order to design and qualify robust automotive electronic components. In a first part, the recent methodologies introduced to screen out extrinsic issues (e.g. misprocess issues) will be presented. Some hints on how to use and to tune accurately the extrinsic failure rate of the components will be given. In a second part, we will introduce design flow elements which are required to design reliable products including reliability models. Dedicated digital and analog design flows are needed to enable reliability-aware design platform. Finally, static and dynamic voltage scaling methodologies will be presented to manage the reliability/energy efficiency trade-off during the useful lifetime. This will enlighten the different parts of the auto-adaptive methodology required from material, devices, cell and blocks, system level till product level robustness.

2. Extrinsic screening

Extrinsic failures are related to misprocess issues. Such misprocess cannot be modelled since they only occur on a stochastic way across production life and thus require to be screened out prior to product shipping to the final customer. This is particularly true in automotive context where final failure rate targeted is below 1 ppm while prime foundry failure rate for extrinsic is in the range of hundreds of ppm. The challenges here rely on achieving the targeted failure rate (below 1 ppm) with a reasonable test time (and thus cost). The first method proposed is called V_{stress} and consists in applying a high voltage for short times at Electrical Wafer Sorting (EWS) level. Correct V_{stress} conditions enable screened failure rate identical to standard Burn-In (BI) failure rate with no impact on intrinsic lifetime (Fig. 3, left). V_{stress} methodology efficiency has been explored experimentally recently by various teams [2–3].

Experimentally, extrinsic failure rate is linked to EWS prime yield. Fundamentally, this relationship is based on the fact that the same types of defects that cause failures at wafer probe can also cause reliability defects. From this perspective, reliability defects, although present at wafer test, are simply not destructive enough to cause a failure. Under

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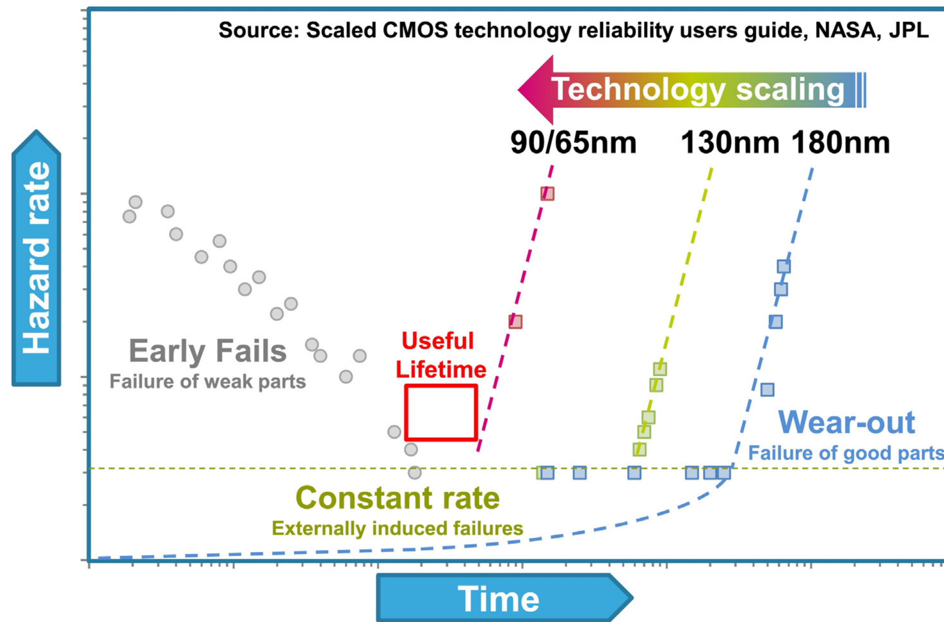

Fig. 1. Bathtub curve and technology scaling.

stress conditions however, such defects can "grow" and become severe enough to cause a circuit failure. Yield to Failure Rate correlation is modelled using Barnett et al. [1] theoretical description (see Fig. 3 left). Chip's local yield is an indicator of chip reliability. This is explained by the fact that defects are not uniformly distributed but have tendency to cluster. A die from a region with many defects (local low yield) will have a larger failure rate then a die coming from local high yield (Fig. 3, right).

The second step in extrinsic screening is the BI. Though conventional BI is applied directly on packaged parts for tens of hours, we have developed a novel approach based on voltage ramp to enable defining wafer-level burn-in (WLBI) conditions to be applied at EWS for tens of seconds [2].

Based on these considerations, it is possible to find WLBI conditions with identical intrinsic impact than standard BI (Fig. 4) and similar screened failure rate (Fig. 5) observed on products with very large sampling up to 1 million (+ parts).

The two-step approach of using both V_{stress} and BI (either conventional or at wafer-level) to screen out extrinsic is now in use for many years and has been proven efficient through field returns analysis. For 51 millions + parts delivered, only 4 silicon fails have been reported which corresponds to 0.1 ppm with 60% confidence limits.

3. Reliability-aware design platform

3.1. Device reliability models

Product reliability margins are often derived from WLR trials using worst-case, physics-of-failure (PoF) approaches. Building up design margins with such approaches in 28 nm nodes generate margins of

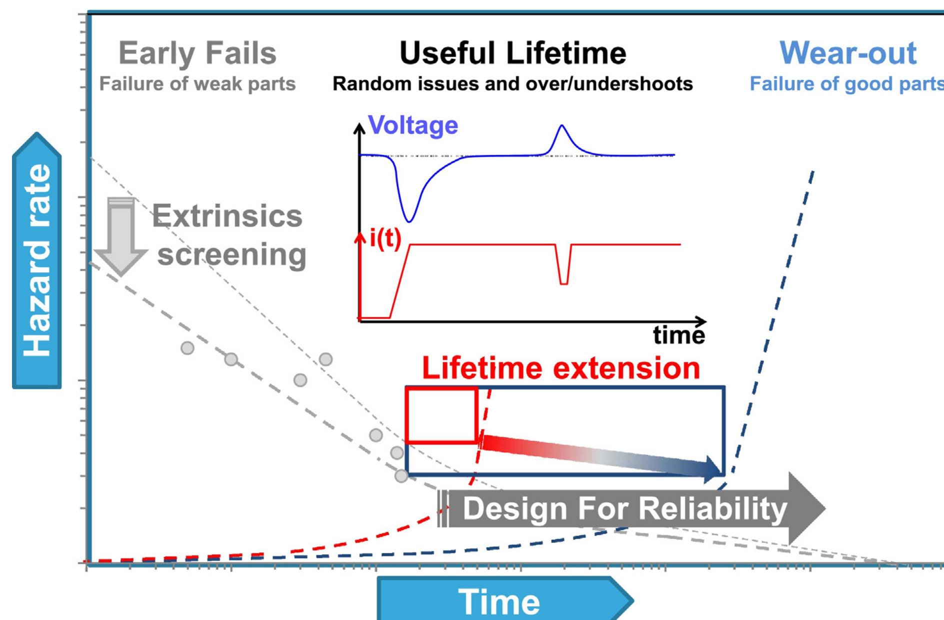

Fig. 2. Managing the bathtub curve through adequate methodologies.

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