Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Analysis of errors in estimating wearout characteristics of time-dependent dielectric breakdown using system-level accelerated life test

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ARTICLE INFO

Article history:
Received 21 May 2017
Received in revised form 10 June 2017
Accepted 20 June 2017
Available online xxxx

ABSTRACT

Reliability issues exacerbated by small feature sizes in modern VLSI circuits challenge an accurate reliability assessment using the conventional approach of employing device-level accelerated life test. Since such device-level reliability assessment ignores tolerance of a circuit or a system to device wearout failures, to accurately estimate circuit/system reliability, we need to directly test a circuit or a system for extraction of wearout parameters in operating environments. In this paper, we propose a system-level accelerated life test to compliment device-level accelerated life test. We also investigate errors in estimating wearout parameters from time-dependent dielectric breakdown (TDDB) from experimental results from system-level accelerated life test and note differences from device-level reliability assessment.

1. Introduction

Reliability issues exacerbated by small feature sizes resulting from continuous technology scaling challenge an accurate reliability assessment using the conventional approach of employing device-level accelerated life test [1]. Since such device-level reliability assessment ignores tolerance of a system to device wearout failure, to accurately estimate system reliability, we need to directly test a system for extraction of wearout parameters in operating environments. In this paper, to accurately characterize system reliability, we propose system-level accelerated life test (ALT) to support device-level accelerated life test. We also investigate errors in estimating wearout parameters from experimental results using system-level ALT.

2. System-level reliability assessment

In a classical approach of estimating system reliability using device-level reliability assessment depicted in Fig. 1, a distribution of a wearout mechanism is extracted from device-level testing, forming a predictive device reliability model. Based on such a device model, a system-level reliability model is built. However, such indirect extraction and estimation of a wearout distribution of a system requires a high reliability margin at the device level [1]. For accurate system reliability assessment, system-level testing is essential.

In prior work [2,3], we proposed a system-level reliability assessment method. Unlike a classical device-level reliability assessment that isolates wearout failures caused by a target wearout mechanism from failures resulting from other wearout mechanisms, the proposed system-level reliability assessment deploys system-level ALT, as illustrated in Fig. 1(b). The BIST scheme distinguishes dissimilar faults, such as shorts vs. opens vs. degradation [4]. Using BIST we isolate system failures due to shorts (such as from time-dependent dielectric breakdown (TDDB)) which is the focus of this work.

Since the purpose of system-level ALT is to directly extract a distribution of each wearout mechanism at the system level for estimating system reliability, in this research, we propose to test a system until we obtain enough data for accurately estimating long-term wearout characteristics, that is, the shape parameter (β) and the characteristic lifetime (η) of a Weibull distribution, commonly used for modelling TDDB wearout, which mainly degrades the reliability of VLSI circuits. Since most TDDB failures in a processor occur in the memory [5], in this research, we investigate memory testing as a case study.

Fig. 1(c) shows a test flow for system-level accelerated life tests using BIST: a system ages while running test patterns, and we periodically test a system with BIST with an interval (t_p) within a test time (t_{limit}). To reduce testing time, we test samples at accelerated test conditions with high voltages and temperatures. As depicted in Fig. 2, we first estimate wearout distributions obtained from system-level accelerated life test. Each test condition provides data for a single linear curve in Fig. 2. Each curve requires the extraction of Weibull parameters (η,β).

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http://dx.doi.org/10.1016/j.microrel.2017.06.039
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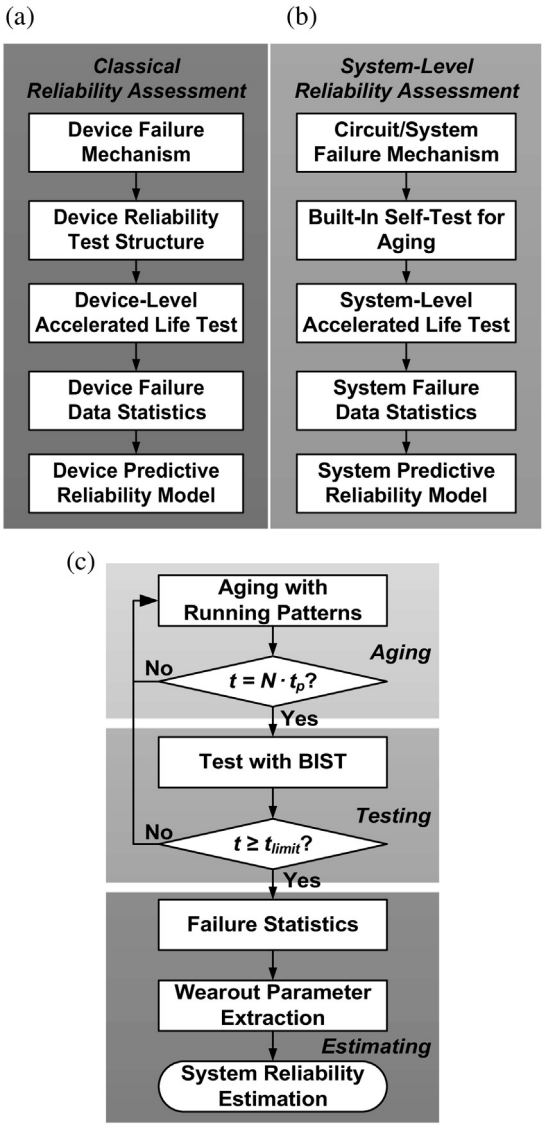

Fig. 1. (a) classical device-level assessment, (b) system-level assessment, and (c) a test flow of system-level ALT [3], where $N = 1, 2, 3, \ldots, \lfloor \frac{t_{limit}}{t_p} \rfloor$ and $\lfloor x \rfloor$ is a floor function of x.

At each test condition, we fit measured data to a Weibull distribution by employing an estimator. Instead of conventional estimating schemes, such as least squares or maximum likelihood regression, for better accuracy of estimation, we employ a generalized maximum likelihood method, which J. Jacquelin proposed in [6] as follows:

$$\eta = \left[\frac{1}{nS_1}\sum_{i=1}^{n} x_i^{\beta}\right]^{\frac{1}{\beta}}, \tag{1}$$

$$\frac{S_2}{\beta} - \frac{\sum_{i=1}^{n} x_i^{\beta} \ln(x_i)}{\sum_{i=1}^{n} x_i^{\beta}} + \frac{1}{n}\sum_{i=1}^{n} \ln(x_i) = 0, \tag{2}$$

where

$$S_1 = \frac{1}{n}\sum_{i=1}^{n} -\ln(1-F_i), \qquad S_2 = \frac{\sum_{i=1}^{n} -\ln(1-F_i)\cdot \ln(-\ln(1-F_i))}{\sum_{i=1}^{n} -\ln(1-F_i)} \tag{3}$$

$$-\frac{1}{n}\sum_{i=1}^{n} \ln(-\ln(1-F_i)). \tag{4}$$

In (1)–(4), the random variable x belongs to a set of data: $x_1, x_2, \ldots, x_i, \ldots, x_n$ from a set of test samples, and F_i denotes the cumulative probability of failure.

After estimating the characteristic lifetime and the shape parameter of a Weibull distribution at accelerated test conditions, since $\log(\eta)$ is regressed linearly to voltages and temperatures, by employing linear regression, we estimate a wearout distribution at the operating conditions.

3. Origins of errors in reliability estimation

We discuss the origins of errors in reliability assessment accounting for not only common errors occurring in both device- and system-level ALT, that is, errors in estimating η, β, and η at the operating conditions (η_{op}), but also a new type of error caused only in system-level ALT, that is, error in estimation of η because of mixed wearout mechanisms.

3.1. Errors in estimating η at accelerated conditions

Fig. 3(a) plots errors in estimating $\log(\eta)$, that is, $\varepsilon_{\log(\eta)}$, with a one-sided 95% confidence interval, calculated using Monte Carlo simulation, with the generalized maximum likelihood method [6] as the estimator. As the shape parameter, β, and the number of samples increase, we have a more accurate estimation of $\log(\eta)$. Note that the number of samples required for testing corresponds to the number of memory cells for system-level memory testing. Hence, it is possible to reduce variation from process parameters by using samples on a single chip, i.e. multiple memory cells within a memory bank. However, in order to observe a sufficient number of failing cells, more extreme accelerated testing is required for a fixed test time.

3.2. Errors in estimating β at accelerated conditions

Fig. 3(b) depicts errors in the estimation of β, that is, ε_{β}, with a one-sided 95% confidence interval generated by Monte Carlo simulation based on a generalized maximum likelihood estimation method [6]. β becomes more accurate with an increased number of samples. However, ε_{β} estimated using the generalized maximum likelihood method estimator is not as accurate as $\log(\eta)$ estimated using the same estimator [7]. Note that the number of samples required for device-level ALT corresponds to the number of failing memory cells in a memory system for system-level ALT. Hence, there must be sufficient acceleration to ensure an adequate number of failing memory cells for the fixed test time.

To enhance the accuracy of estimating ε_{β}, B. P. Linder et al. deployed an estimation of β based on area scaling [8]. For the use of area scaling, we require two groups of test samples with the same number of

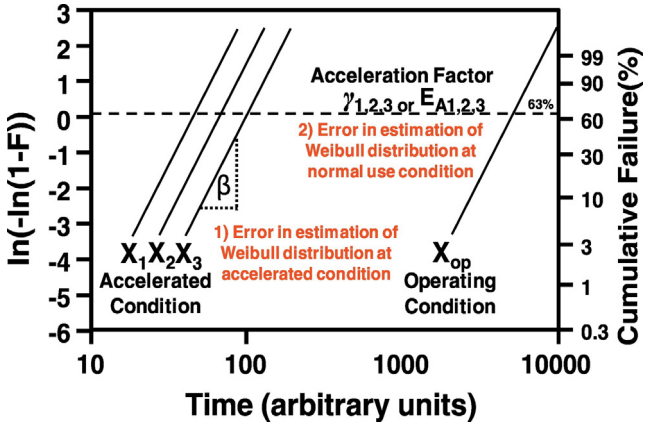

Fig. 2. Errors in estimating Weibull distribution at the operating condition using system-level accelerated life test: (1) errors in the estimation of Weibull parameters at accelerated condition and (2) errors in the estimation of acceleration factors.

Please cite this article as: D.-H. Kim, L. Milor, Analysis of errors in estimating wearout characteristics of time-dependent dielectric breakdown using system-level accelerated lif..., Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2017.06.039