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Method for evaluation of transient-fault detection techniques

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ABSTRACT

This work introduces a simulation-based method for evaluating the efficiency of detection techniques in identifying transient faults provoked in combinational logic blocks. Typical fault profiles are simulated in campaigns of injections that reproduce output scenarios of fault-affected combinational circuits. Furthermore, a detection technique is proposed and compared to state-of-the-art strategies by using the method presented herein. Results show the capabilities of all studied techniques, providing a rank in terms of their efficiencies in detecting transient faults induced in combinational logic circuits, and analyzing the situations in which soft errors are produced in memory elements.

1. Introduction

With the downscale of integrated circuits components, increasing their robustness against various natural or human aggressions is becoming a challenging task. Among natural aggressions, one can identify aging or environmental radiations [1]. Among human aggressions one can cite fault injection to the end of disabling embedded security protocols or mechanisms [2]. Several phenomena such as radiation exposure and many others caused by environmental conditions are able to induce parasitic transient currents in integrated circuits. Intentional sources, such as laser beams can also be used, since it allows finely controlling the injected transient faults thanks to the high spatial and temporal resolutions of laser shots [3]. Transient faults (TFs) are active only for a short duration of time and their occurrence are not predictable when caused by the environment. Therefore, TFs must be detected and corrected at runtime before becoming a soft error (SE) that may affect the operation of the target. Error detection during circuit normal operation is typically called concurrent error detection (CED) [4].

Several CED techniques have been proposed with the intent to design reliable computing systems [5–13]. These techniques mainly differ in their detection capabilities and in the constraints they impose on the system design.

This paper presents a simulation-based method to evaluate and compare different detection techniques regarding their efficiency in detecting TFs arisen in combinational logic blocks and resulting in soft errors. The method proposes 32 different scenarios of TF injection. Results of all detection techniques studied here are summarized in a table that provides a direct insight of the efficiency of each technique. Furthermore, in this paper, another CED technique is introduced and compared among the other techniques. It uses an efficient transition detector (TD) and a controllable adaptive detection window (DW). As a result, the introduced technique offers increased SE detection capability but also allows the detection of delay errors (DEs).

2. Techniques for concurrent error detection

The CED techniques presented in this section can be clustered in three categories: spatial redundancy, temporal redundancy, and techniques based on the integration of a transition detector. Although these approaches can be implemented at different abstraction levels of the design flow, this work considers only the hardware (transistor) abstraction level.

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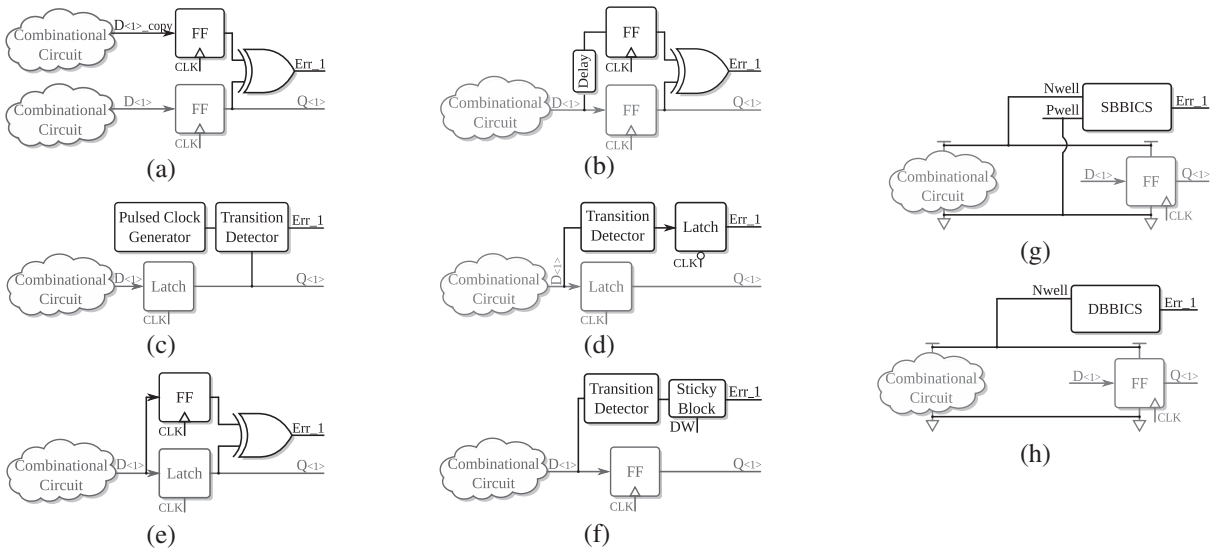

Fig. 1. CED: (a) DWC [5], (b) TR [6], (c) Razor-II [8], (d) TDTB [9], (e) DSTB [9], (f) TFMS [13], (g) SBBICS [12], (h) DBBICS [11].

2.1. Duplication with comparison (DWC)

The DWC method [5] is illustrated in Fig. 1 (a). It is conceptually the simplest error detection method. As shown, it is based on the concept of spatial redundancy. The outputs $D_{<1>}$ and $D_{<1>}copy$ (duplication of the circuit's logic) are connected to two D-type flip-flops (DFFs) whose outputs are compared to generate an error signal.

2.2. Time redundancy (TR)

The TR scheme [6] (see Fig. 1 (b)) uses time redundancy in order to repeat the same computation with the same hardware at different times. The output of the two DFFs are compared, and, if the outputs are divergent, the error signal is raised.

2.3. RAZOR-II

Razor-II [8] is a TD-based technique to detect among other faults, the advent of SEs. A simplified circuit diagram of this scheme is shown in Fig. 1 (c). The design assumption is that the output of the latch may only change shortly after the rising edge of the clock. A TD block is added at the output of the latch in order to detect TFs. To avoid false error signaling, a short negative pulse on DC is used to disable the TD for at least the duration of the clock-to-Q delay after the rising edge.

2.4. Transition detector with time borrowing (TDTB)

The TDTB [9] is similar to Razor-II. It consists in the coupling of a latch and a TD as illustrated in Fig. 1 (d). The transition detector raises the error signal for any input transitions during the low state of the clock ($C\bar{L}K$), thus requiring the signal $D_{<1>}$ to be stable before the low period of the clock.

2.5. Double sampling with time-borrowing (DSTB)

The DSTB [9] presented in Fig. 1 (e) is similar to TDTB although a shadow flip-flop replaces the transition detector. DSTB double samples signal $D_{<1>}$ and compares the latch and shadow flip-flop outputs to generate the error signal. Furthermore, DSTB retains the time-borrowing feature of TDTB to eliminate data-path metastability.

2.6. Transient fault monitoring scheme (TFMS)

The TFMS proposed in [13] detects TFs affecting the DFF input such as signal $D_{<1>}$. As shown in Fig. 1 (f), this scheme includes a *transition detector*, which generates a high signal when there is a TF inside the *detection window* (signal "DW"). The *sticky block* is used to validate TFs occurring only inside the DW and to merge the error signal since the TD produces two pulses.

2.7. Single bulk built-in current sensor (SBBICS)

A BBICS [10] is designed to monitor the induced transient currents passing through the bulk of transistors, these currents are induced by radiation or laser illumination. The SBBICS architecture allows monitoring simultaneously the pull-up and pull-down of CMOS networks [12] as conceptually shown in Fig. 1 (g).

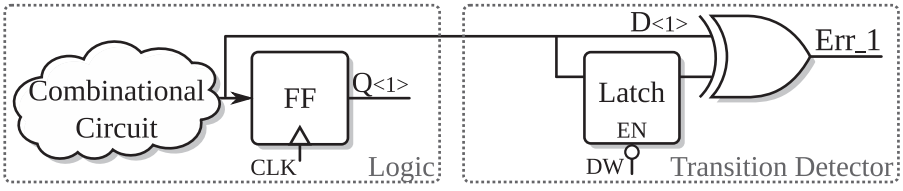

Fig. 2. The proposed scheme for detecting TF that results in illegal transitions at combinational circuit's outputs like the bit $D_{<1>}$.

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