Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Characterization of Low Drop-Out during ageing and design for yield

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ARTICLE INFO

Article history:
Received 21 May 2017
Received in revised form 3 July 2017
Accepted 8 July 2017
Available online xxxx

ABSTRACT

Low Drop-Out (LDO) voltage regulators are extensively used to provide a stable power supply voltage independent of load impedance. LDO must be robust with regard to input voltage, temperature and local mismatch variations. Moreover, it must fulfill these specifications all along its lifetime. The influence of process variation on LDO performances has intensively been studied, but only few works are reported about ageing mechanisms. This paper presents an illustrative case study on the change of LDO performances due to wear-out mechanisms. The ageing effects are investigated on the static and dynamic performances parameters. After introducing LDO design content, a review of degraded performances (Output Voltage VOUT, Power Supply Rejection Ratio (PSRR), shutdown current…) is presented and compared to simulation. Then, statistical VOUT measurements are presented and compared with Monte Carlo simulations. Finally, sizing for yield methodology is introduced. The objective is to find optimal device size to guarantee a target of failure rate in fresh and aged conditions.

1. Reliability of LDO

Low Drop-Out (LDO) voltage regulator is a DC linear voltage regulator which is mainly based on a negative feedback control loop, a power pass device and an output capacitor C_{OUT} as shown in the block diagram of Fig. 1. The voltage regulation is done through a negative feedback loop formed by the voltage divider (R1 and R2) and the high gain error amplifier. The regulator ensures a constant output voltage V_{OUT} whatever the output current requested by the output load. The LDO is designed to minimize the voltage drop between the supply voltage V_{DD} and the output voltage V_{OUT}. The main features to be considered for LDO are: drop-out voltage, DC load regulation, shutdown and ground currents, load/line regulation, load/line transient and Power Supply Rejection Ratio (PSRR) [1,2].

As illustrated in Fig. 2, LDO regulators operate in three different regions: linear region (feedback loop regulates V_{out}), dropout region (the circuit still operates but with little feedback), and off region (the circuit no longer regulates V_{out}). Below VDropout, the output voltage falls rapidly with decreasing input voltages. In the dropout region, the pass device acts like a resistor with a value equal to the drain-to-source on resistance of the MOS transistor (RDS_{ON}).

Recent works have reported that LDO can suffer from reliability issues and performance drifts are observed after electrical accelerated ageing [3]. In order to investigate the robustness of LDO to process variation and ageing, a general purpose LDO (Fig. 3) has been designed in 28 nm FDSOI technology from STMicroelectronics with thick oxide devices. This LDO is designed to supply an output voltage V_{OUT} of 1.5 V with a dropout about 300 mV and a maximum output current of 100 μA as shown in Fig. 4. The circuit is studied with an external load circuitry.

The regulation functionality is evaluated in Fig. 4. As expected, it gets worse when the load current I_{load} increases because the LDO's overall loop gain decreases. In the linear region, regulation is effective with a decreasing efficiency at higher supply voltage (higher LDO's power dissipation when the supply-to-output voltage difference increases). This power dissipation causes the rising of junction temperature, inducing some band-gap voltage and internal offset voltage drops.

Concerning the reliability, an intensive device characterization in terms of Hot Carrier Injection (HCI) at wafer level has been done and ageing models have been developed [4,5]. The I_{on} drift (VDS = VGS = 1.8) is measured during DC stress. As depicted in Fig. 5, drift for different stress (NMOS thick oxide) and projection at nominal condition are reported. These models are used to perform Design-in-Reliability simulations. Then, measurements were carried out at different test points and after typical AC stress with duration of 3 h at high temperature.

AC signal is 50% duty cycle with 2 μs period. The signal is composed of I_{load} at 300 μA (50% of time) and 50% of time the LDO is in linear region.

The LDO capability to maintain the specified output voltage of V_{out} = 1.5 V under varying load conditions from 1 nA to 1 mA is checked during stress conditions. Load regulation is measured, as shown in Figs. 6 and 7 after different stress levels. For an AC stress at 125 °C, the LDO maintains the targeted output voltage 1.5 V up to I_{load} = 400 μA. For an AC stress at 165 °C, the maximal load current goes down to 300 μA. A variation of ± 10% in V_{DD} at 165 °C leads to a shift of ± 60% of I_{load}. After stress, the drop-out region shifts about

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http://dx.doi.org/10.1016/j.microrel.2017.07.047
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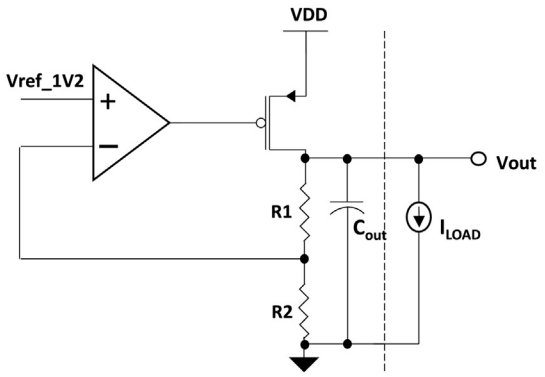

Fig. 1. Simplified schematic of low-dropout regulator. The LDO is investigated with external load circuitry.

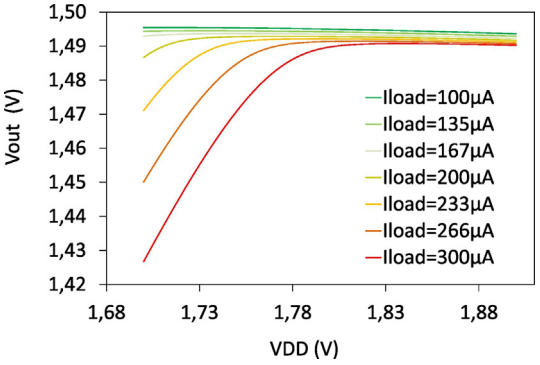

Fig. 4. Regulated voltage V_{out} in function of I_{load}. In nominal condition, the DC regulation is specified for 100 µA of current load.

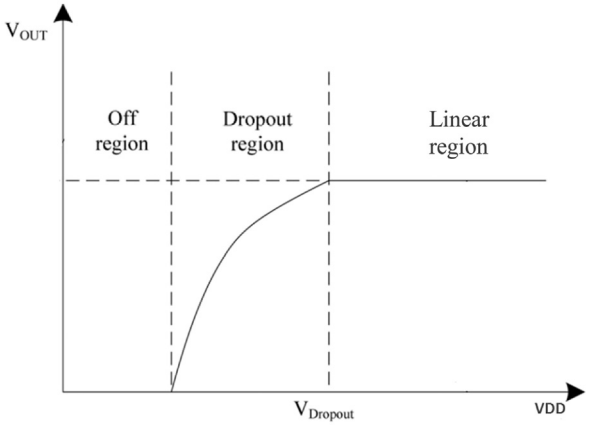

Fig. 2. Typical VDD/VOUT voltage characteristics of LDO.

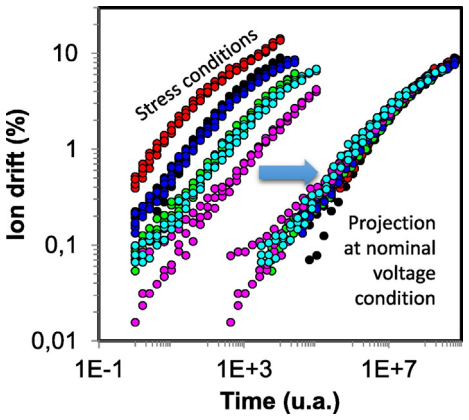

Fig. 5. HCI stress condition for thick oxide NMOS 28 nm FDSOI device.

30 mV and 40 mV for respectively 125 °C and 165 °C. The linear region has shifted for 8 mV and 10 mV for respectively 125 °C and 165 °C. This shift is mainly due to the ageing of the MOS transistors used in the differential pair of the amplifier (N3, N4 on Fig. 3) and to the ageing of the PMOS pass transistor (P4 on Fig. 3) as confirmed by sensitivity analysis (Fig. 14)

Another LDO feature is the shutdown current which is the supply current drawn by the LDO when the output is disabled. The error amplifier is not powered in shutdown mode. As shown in Fig. 8, the shutdown current increases with temperature, due to higher leakage currents. When comparing fresh and aged states, the $I_{shutdown}$ was reduced, thanks to the PMOS pass device (P4) having a higher threshold voltage V_{TH} and a worse I_{off} after ageing. Qualitative agreement with simulation is observed at 165 °C in Fig. 8.

The ground current is the difference between the input and output currents. Measurement and simulation for different I_{load} from 1 nA to 1 mA at 165 °C and $V_{DD} = 1.8$ V are reported in Fig. 9. The ground current I_{GND} increases with the load current because the gate voltage driving the PMOS pass device (P4) has to increase to compensate for the voltage drop. After ageing, the ground current presents the same behaviour with a negative offset compared to the fresh one. Quantitative agreement with simulation is observed (Fig. 9).

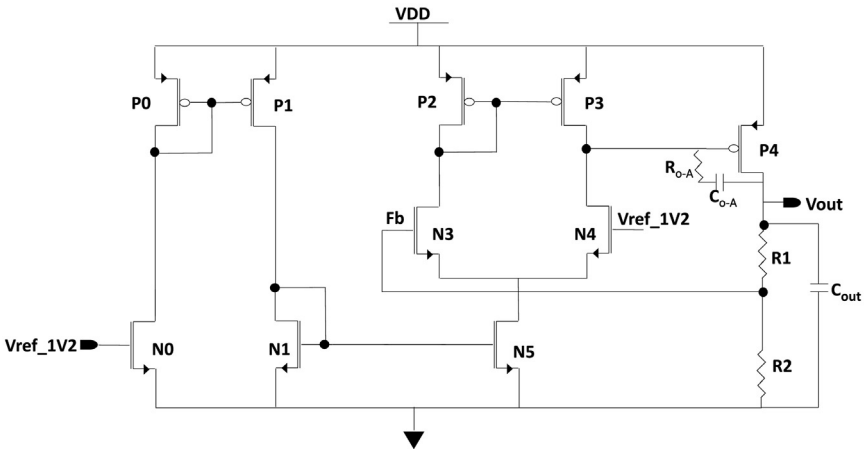

Fig. 3. Schematic of LDO using PMOS output device and conventional operational transconductance amplifier.

Please cite this article as: R. Lajmi, et al., Characterization of Low Drop-Out during ageing and design for yield, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.07.047